19-2569; Rev 0; 10/02

MAXIM

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

General Description

The MAX1816/MAX1994 are dual step-down controllers for notebook computer applications. BUCK1 is a CPU core regulator with dynamically adjustable output, ultra-fast transient response, high DC accuracy, and high efficiency. BUCK2 is an adjustable step-down regulator for I/O and memory supplies. Both regulators employ Maxim's proprietary Quick-PWM™ control architecture. This fast-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant" on-response to load transients, while maintaining a relatively constant switching frequency. The MAX1816/MAX1994 also have a linear-regulator controller for low-voltage auxiliary power supplies.

The CPU regulator supports "active voltage positioning" to reduce output bulk capacitance and lower power dissipation. A programmable gain amplifier allows the use of lower value sense resistors. Four fixed-gain settings are available (0, 1.5, 2, and 4). A differential remote-sense amplifier is also included to more accurately control the voltage at the load. Accuracy is further enhanced with an internal integrator.

The MAX1816/MAX1994 include a specialized digital interface that makes them suitable for mobile CPU and video processor applications. The power-good (PGOOD) output for the core regulator is forced high during VID transitions, and the LINGOOD output for the linear regulator includes a 1ms (min) turn-on delay.

BUCK1, BUCK2, and the linear regulator feature overvoltage protection (OVP). The detection threshold for BUCK1 is adjusted with an external resistive voltage-divider, while the OVP thresholds for BUCK2 and the linear regulator are fixed. Connecting the OVPSET pin to V_{CC} disables OVP for BUCK1 and BUCK2, but not the linear regulator.

The MAX1816 features an output-voltage adjustment range from 0.6V to 1.75V. Similarly, the MAX1994 is adjustable from 0.925V to 2.0V, using an alternate VID code set. While in suspend mode, the adjustment range is 0.7V to 1.075V for both the MAX1816 and MAX1994. Both parts are available in 48-pin thin QFN packages.

Applications

Mobile CPU Core and Video Processors

Memory I/O and VID Supplies

3- to 4-Cell Li+ Battery to CPU Core Supply

Small Notebook Computers

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

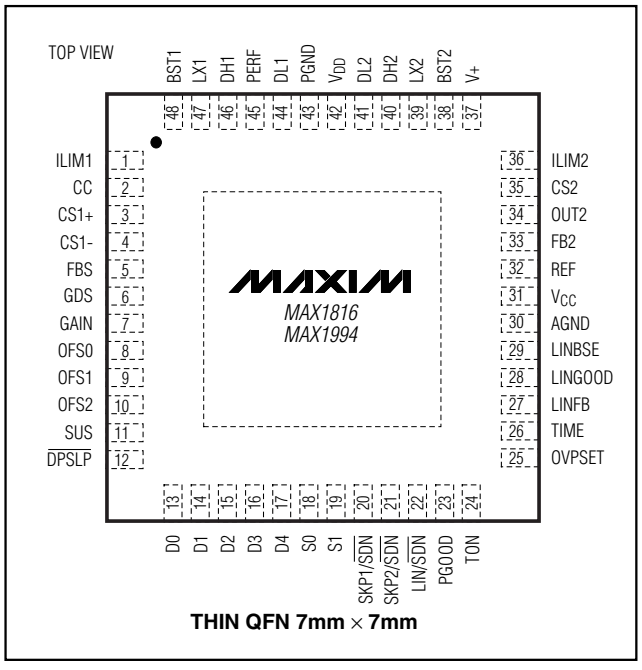
Features

- **Dual Quick-PWM Architecture**
- **±1% V_{OUT} Accuracy**
- **5-Bit On-Board D/A Converter**
- **+0.60V to +1.75V Output Adjust Range (MAX1816)**
- **+0.70V to +2.00V Output Adjust Range (MAX1994)**
- **Voltage-Positioning Gain and Offset Control**
- **+2V to +28V Battery Input Range**
- **Differential Remote Sense (BUCK1)**
- **Linear-Regulator Controller**
- **200/300/550/1000kHz Switching Frequency**
- **2.2mA (typ) I_{CC} Supply Current**
- **20µA (max) Shutdown Supply Current**
- **Independent Power-Good Outputs (PGOOD, LINGOOD)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1816ETM	-40°C to +100°C	48 Thin QFN
MAX1994ETM	-40°C to +100°C	48 Thin QFN

Pin Configuration



THIN QFN 7mm × 7mm

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

V+ to AGND .....-0.3V to +30V
V_{CC}, V_{DD} to AGND .....-0.3V to +6V
PGND, GDS to AGND .....±0.3V
SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$, LIN/$\overline{SDN}$ to AGND .....-0.3V to +16V
LINBSE, SUS, PERF, $\overline{DPSLP}$, PGOOD,
LINGOOD, CS1+, CS1-, FBS, D0–D4,
OUT2 to AGND .....-0.3V to +6V
OFS0, OFS1, OFS2, ILIM1, ILIM2,
FB2, REF, TON, TIME, OVPSET, S0, S1,
GAIN, CC, LINFB to AGND .....-0.3V to (V_{CC} + 0.3V)
DL1, DL2 to PGND .....-0.3V to (V_{DD} + 0.3V)
DH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
DH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
BST1 to LX1 .....-0.3V to +6V
BST2 to LX2 .....-0.3V to +6V
LX1, LX2, CS2 to AGND .....-2V to +30V
REF Short Circuit to AGND .....Continuous
LINBSE Short Circuit to +6V .....Continuous
Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derate 26.3mW/°C above +70°C) .2105mW
Operating Temperature Range .....-40°C to +100°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	Battery voltage V+	TON = REF, open, or V_{CC}	2		28	V
		TON = GND	2		16	
	V_{CC}, V_{DD}		4.5		5.5	
BUCK1 DC Output Voltage Accuracy	V+ = 4.5V to 28V, includes load regulation errors, OFS_ = GDS = AGND, CS1+ = CS1- = FBS	DAC codes from 0.600V to 1.750V (MAX1816)	-1		+1	%
		DAC codes from 0.700V to 2.000V (MAX1994)				
BUCK2 Error Comparator Threshold (DC Output Voltage Accuracy) (Note 1)	V+ = 4.5V to 28V	FB2 = GND	2.475	2.500	2.525	V
		FB2 = V_{CC}	1.782	1.800	1.818	
		FB2 = OUT2	0.990	1.000	1.010	
OUT2 Adjust Range			1.0		5.5	V
FB2 GND Level	Voltage level to enable internal feedback for BUCK2 with V_{OUT2} = 2.5V				0.05	V
FB2 External Feedback Level	Voltage level to enable external feedback for BUCK2 with FB2 regulated to 1.0V nominal		0.15		1.90	V
FB2 V_{CC} Level	Voltage level to enable internal feedback for BUCK2 with V_{OUT2} = 1.8V		2.10			V
Voltage-Positioning Gain	GAIN = GND			0		V/V
	GAIN = REF		1.425	1.500	1.575	
	GAIN = open		1.900	2.000	2.100	
	GAIN = V_{CC}		3.800	4.000	4.200	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Sense Differential Input Range (CS1+, CS1-)					200	mV
Remote-Sense Differential Input Range (CS1+, FBS)					300	mV
Remote-Sense Differential Input Range (GDS, AGND)					200	mV
CS1+, FBS Input Bias Current	-300mV < V_{CS1+} - V_{FBS} < +300mV		-60		+60	µA
CS1- Input Bias Current	-100mV < V_{CS1+} - V_{CS1-} < +100mV, V_{CS1-} = V_{FBS}		-60		+60	µA
GDS Input Bias Current			-3		+3	µA
FB2 Input Bias Current			-0.2		+0.2	µA
OUT2 Input Resistance			70			kΩ
TIME Frequency Accuracy	252kHz nominal, R_{TIME} = 143kΩ		-8		+8	%
	53kHz nominal to 530kHz nominal, R_{TIME} = 680kΩ to 68kΩ		-12		+12	
BUCK1 On-Time (Note 2)	V+ = 5V, CS1- = 1.2V	TON = GND (1000kHz)	230	260	290	ns
	V+ = 12V, CS1- = 1.2V	TON = REF (550kHz)	165	190	215	
		TON = open (300kHz)	320	355	390	
		TON = V_{CC} (200kHz)	465	515	565	
BUCK2 On-Time (Note 2)	V+ = 5V, OUT2 = 2.5V	TON = GND (715kHz)	630	720	810	ns
	V+ = 12V, OUT2 = 2.5V	TON = REF (390kHz)	495	550	605	
		TON = open (390kHz)	495	550	605	
		TON = V_{CC} (260kHz)	740	825	910	
Minimum Off-Time	TON = open, TON = V_{CC} (Note 2)			425	500	ns
	TON = GND, TON = REF (Note 2)			325	375	
Quiescent Supply Current (V_{CC})	Measured at V_{CC}, with FBS, OUT2, FB2, and LINFB forced above the no-load regulation point			2200	3800	µA
Partial Shutdown Supply Current (Linear Regulator On Only)	$V_{SKP1/\overline{SDN}}$ = 0V, $V_{SKP2/\overline{SDN}}$ = 0V, $V_{LIN/\overline{SDN}}$ = 5V; measured at V_{CC}, with FBS and LINFB forced above the no-load regulation point			425	650	µA
Partial Shutdown Supply Current (BUCK1 and Linear Regulator)	$V_{SKP1/\overline{SDN}}$ = 5V, $V_{SKP2/\overline{SDN}}$ = 0V, $V_{LIN/\overline{SDN}}$ = 5V; measured at V_{CC}, with FBS and LINFB forced above the no-load regulation point			1825	3000	µA
Partial Shutdown Supply Current (BUCK2 Only)	$V_{SKP1/\overline{SDN}}$ = 0V, $V_{SKP2/\overline{SDN}}$ = 5V, $V_{LIN/\overline{SDN}}$ = 0V; measured at V_{CC}, with OUT2 and FB2 forced above the regulation point			600	1100	µA
Quiescent Supply Current (V_{DD})	Measured at V_{DD}, with FBS, OUT2, and FB2 forced above the no-load regulation point			<1	5	µA

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Battery Current	Measured at V+			25	40	µA
Shutdown Supply Current (V_{CC})	$V_{SKP1/\overline{SDN}}$ = 0V, $V_{SKP2/\overline{SDN}}$ = 0V, and $V_{LIN/\overline{SDN}}$ = 0V			4	10	µA
Shutdown Supply Current (V_{DD})	$V_{SKP1/\overline{SDN}}$ = 0V, $V_{SKP2/\overline{SDN}}$ = 0V, and $V_{LIN/\overline{SDN}}$ = 0V			<1	5	µA
Shutdown Battery Current	$V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = 0V, measured at V+, with V_{CC} = V_{DD} = 0V or 5V			<1	5	µA
Reference Voltage	V_{CC} = 4.5V to 5.5V, I_{REF} = 50µA sourcing		1.98	2.00	2.02	V
Reference Load Regulation	I_{REF} = 0 to 50µA		0		7	mV
	I_{REF} = 50µA to 100µA		0		7	
Reference Sink Current	REF in regulation		10			µA
OVPSET Disable Mode Threshold	Voltage at OVPSET above which the OVP functions are disabled for BUCK1 and BUCK2		V_{CC} - 1.5		V_{CC} - 0.5	V
OVPSET Default Mode Threshold for BUCK1	Voltage at OVPSET below which the OVP thresholds are set to their default values		0.4		0.6	V
Overvoltage Trip Threshold for BUCK1 (Fixed OVP Threshold)	OVPSET = GND, measured at FBS	MAX1816	1.95	2.00	2.05	V
		MAX1994	2.20	2.25	2.30	
Overvoltage Trip Threshold for BUCK1 (Adjustable Threshold)	V_{OVPSET} = 1.0V, measured at FBS	MAX1816	0.95	1.00	1.05	V
		MAX1994	1.075	1.125	1.175	
	V_{OVPSET} = 2.0V, measured at FBS	MAX1816	1.95	2.00	2.05	
		MAX1994	2.20	2.25	2.30	
Overvoltage Trip Threshold for BUCK2	Measured at OUT2 (or FB2 if external feedback is used)		113	115	117	%
OVPSET Bias Current	0V < V_{OVPSET} < V_{CC}		-100		+100	nA
Overvoltage Fault Propagation Delay	FBS, OUT2, FB2, and LINFB forced 2% above the no-load trip threshold			10		µs
Output Undervoltage Protection Threshold	With respect to unloaded output voltage, FBS, and OUT2 (FB2 in external feedback)		65	70	75	%
Output Undervoltage Fault Propagation Delay	FBS, OUT2, FB2, and LINFB forced 2% below trip threshold			10		µs
Output Undervoltage Protection Blanking Time for FBS	From SKP1/$\overline{SDN}$ signal going high; clock speed set by R_{TIME} (Note 3)			256		Clks
Output Undervoltage Protection Blanking Time for OUT2	From SKP2/$\overline{SHDN}$ signal going high; clock speed set by R_{TIME} (Note 3)			4096		Clks
Linear Regulator (LINFB) Undervoltage Protection Blanking Time	Linear regulator; from LIN/$\overline{SDN}$ signal going high; clock speed set by R_{TIME} (Note 3)			512		Clks

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ILIM1 Default Threshold		V_{CC} - 1.5	V_{CC} - 1.0	V_{CC} - 0.5	V
BUCK1 Current-Limit Threshold (Fixed)	CS1+ - CS1-; V_{ILIM1} = V_{CC}	40	50	60	mV
BUCK1 Current-Limit Threshold (Adjustable)	CS1+ - CS1-; V_{ILIM1} = 0.5V	40	50	60	mV
	CS1+ - CS1-; V_{ILIM1} = 2.0V	160	200	240	
BUCK1 Negative Current-Limit Threshold (Fixed)	CS1+ - CS1-; V_{ILIM1} = V_{CC}	-90	-72	-55	mV
ILIM1 Input Bias Current	0 to 2V	-100		+100	nA
CS2 Input Bias Current	0 to 28V	-1		+1	µA
ILIM2 Default Threshold		V_{CC} - 1.5	V_{CC} - 1.0	V_{CC} - 0.5	V
BUCK2 Current-Limit Threshold (Fixed)	AGND - CS2; V_{ILIM2} = V_{CC}	40	50	60	mV
BUCK2 Current-Limit Threshold (Adjustable)	AGND - CS2; V_{ILIM2} = 0.5V	40	50	60	mV
	AGND - CS2; V_{ILIM2} = 2.0V	160	200	240	
BUCK2 Negative Current-Limit Threshold (Fixed)	AGND - CS2; V_{ILIM2} = V_{CC}	-90	-72	-55	mV
ILIM2 Input Bias Current	0 to 2V	-100		+100	nA
Thermal-Shutdown Threshold	15°C hysteresis		160		°C
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV	4.10		4.45	V
DH1 Gate-Driver On-Resistance	BST1–LX1 forced to 5V (Note 4)		1	4.5	Ω
DL1 Gate-Driver On-Resistance	DL1 high state (pullup) (Note 4)		1	4.5	Ω
	DL1 low state (pulldown) (Note 4)		0.35	2	
DH1 Gate-Driver Source/Sink Current	DH1 forced to 2.5V, BST–LX forced to 5V		1.5		A
DL1 Gate-Driver Sink Current	DL1 forced to 2.5V		5		A
DL1 Gate-Driver Source Current	DL1 forced to 2.5V		1.5		A
Dead Time	DL1 rising		35		ns
	DH1 rising		26		
DH2 Gate-Driver On-Resistance	BST2–LX2 forced to 5V (Note 4)		2	8	Ω
DL2 Gate-Driver On-Resistance	DL2 high state (pullup) (Note 4)		2	8	Ω
	DL2 low state (pulldown) (Note 4)		0.7	3	

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DH2 Gate-Driver Source/Sink Current	DH2 forced to 2.5V, BST2–LX2 forced to 5V		0.75		A
DL2 Gate-Driver Sink Current	DL2 forced to 2.5V		2.5		A
DL2 Gate-Driver Source Current	DL2 forced to 2.5V		0.75		A
Dead Time	DL2 rising		35		ns
	DH2 rising		26		
LINFB Input Bias Current	V_{LINFB} = 1.035V	-100		+100	nA
LINBSE Drive Current	V_{LINFB} = 1.05V, V_{LINBSE} = 5V			0.4	mA
	V_{LINFB} = 0.965V, V_{LINBSE} = 0.5V	20			
LINFB Regulation Voltage	V_{LINBSE} = 5V, I_{LINBSE} = 4mA (sink)	0.988	1.000	1.017	V
LINFB Load Regulation	V_{LINBSE} = 5V, I_{LINBSE} = 2mA to 10mA (sink)	-2.2	-1.2		%
Logic Input High Voltage	D0–D4, SUS, PERF, LIN/$\overline{SDN}$	2.4			V
Logic Input Low Voltage	D0–D4, SUS, PERF, LIN/$\overline{SDN}$			0.8	V
Logic Input High Voltage	$\overline{DPSLP}$	0.8			V
Logic Input Low Voltage	$\overline{DPSLP}$			0.4	V
Logic Input Current	D0–D4, SUS, PERF, LIN/$\overline{SDN}$, $\overline{DPSLP}$ = 0V or 5V	-1		+1	µA
Four-Level Logic V_{CC} Level	TON, S0, S1, GAIN logic input high level	V_{CC} - 0.4			V
Four-Level Logic Float Level	TON, S0, S1, GAIN logic input upper midlevel	3.15		3.85	V
Four-Level Logic REF Level	TON, S0, S1. GAIN logic input lower midlevel	1.65		2.35	V
Four-Level Logic GND Level	TON, S0, S1, GAIN logic input low level			0.5	V
SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$, S0, S1, GAIN, and TON Logic-Input Current	SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$, TON, S0, S1, GAIN forced to GND or V_{CC}	-3		+3	µA
SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ Skip Level	SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ logic input high level	2.8			V
SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ PWM Level	SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ logic input float level	1.4		2.2	V
SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ Shutdown Level	SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ logic input low level			0.4	V
SKP1/$\overline{SDN}$ Test Mode Input Voltage Range	To enable no-fault mode, 4.5V < V_{CC} < 5.5V	10.8		13.2	V
PGOOD Lower Trip Threshold	Measured at FBS, OUT2, and FB2 with respect to unloaded output voltage, falling edge, typical hysteresis = 1%	-12.0	-10.0	-8.0	%
LINGOOD Lower Trip Threshold and LINFB Undervoltage Protection Threshold	Measured at LINFB with respect to unloaded output voltage, falling edge (Note 5)	-12.0	-10.0	-8.0	%
PGOOD Upper Trip Threshold	Measured at FBS, OUT_, FB2 with respect to unloaded output voltage, rising edge, typical hysteresis = 1%	8.0	10.0	12.0	%

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LINGOOD Upper Trip Threshold and LINFB Overvoltage Trip Threshold	Measured at LINFB with respect to unloaded output voltage, rising edge (Note 5)	8.0	10.0	12.0	%
PGOOD Propagation Delay	OUT_, FB2 forced 2% above or below PGOOD trip threshold		10		µs
LINGOOD Turn-On Delay	LINFB forced 2% above LINGOOD lower trip threshold	1			ms
LINGOOD Turn-Off Delay	LINFB forced 2% below LINGOOD lower trip threshold		10		µs
PGOOD Transition Delay	After the output-voltage transition on BUCK1 is complete (PGOOD blanking is enabled for N + 4 clocks, blanking is excluded in startup and shutdown)		4		Clk
Forced-PWM Mode Transition Delay	After the output-voltage transition on BUCK1 is complete (forced-PWM mode persists for N + 32 clocks for all transitions)		32		Clk
Open-Drain Output Low Voltage (PGOOD, LINGOOD)	I_{SINK} = 3mA			0.4	V
Open-Drain Leakage Current (PGOOD, LINGOOD)	High state, forced to 5.5V			1	µA
Input Current	OFS0–OFS2	-0.1		+0.1	µA
OFS Positive Offset when Programmed to Zero	Deviation in the output voltage when tested with OFS_ connected to REF			2	mV
OFS Gain	ΔV_{OUT} / ΔV_{OFS}, ΔV_{OFS} = (0.8V - 0V)	0.119	0.125	0.131	V/V
	ΔV_{OUT} / ΔV_{OFS}, ΔV_{OFS} = (2.0V - 1.2V)	0.119	0.125	0.131	

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = -40°C to +100°C**, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	Battery voltage V+	TON = REF, open, or V_{CC}	2		28	V
		TON = GND	2		16	
	V_{CC}, V_{DD}		4.5		5.5	
BUCK1 DC Output-Voltage Accuracy	V+ = 4.5V to 28V, includes load regulation errors, OFS_ = GDS = AGND, CS1+ = CS1- = FBS	DAC codes from 0.600V to 1.750V (MAX1816)	-1.5		+1.5	%
		DAC codes from 0.700V to 2.000V (MAX1994)				
BUCK2 Error Comparator Threshold (DC Output-Voltage Accuracy) (Note 1)	V+ = 4.5V to 28V	FB2 = GND	2.463		2.538	V
		FB2 = V_{CC}	1.773		1.827	
		FB2 = OUT2	0.985		1.015	
OUT2 Adjust Range			1.0		5.5	V
Voltage-Positioning Gain	GAIN = REF		1.425		1.575	V/V
	GAIN = open		1.900		2.100	
	GAIN = V_{CC}		3.800		4.200	
Current-Sense Differential Input Range (CS1+, CS1-)					200	mV
Remote-Sense Differential Input Range (CS1+, FBS)					300	mV
Remote-Sense Differential Input Range (GDS, AGND)					200	mV
CS1+, FBS Input Bias Current	-300mV < V_{CS1+} - V_{FBS} < +300mV		-60		+60	µA
CS1- Input Bias Current	-100mV < V_{CS1+} - V_{CS1-} < +100mV, V_{CS1-} = V_{FBS}		-60		+60	µA
TIME Frequency Accuracy	252kHz nominal; R_{TIME} =143kΩ		-8		+8	%
	53kHz nominal to 530kHz nominal; R_{TIME} = 680kΩ to 68kΩ		-12		+12	
BUCK1 On-Time (Note 2)	V+ = 5V, CS1- = 1.2V	TON = GND (1000kHz)	230		290	ns
	V+ = 12V, CS1- = 1.2V	TON = REF (550kHz)	165		215	
		TON = open (300kHz)	320		390	
		TON = V_{CC} (200kHz)	465		565	
BUCK2 On-Time (Note 2)	V+ = 5V, OUT2 = 2.5V	TON = GND (715kHz)	630		810	ns
	V+ = 12V, OUT2 = 2.5V	TON = REF (390kHz)	495		605	
		TON = open (390kHz)	495		605	
		TON = V_{CC} (260kHz)	740		910	
Minimum Off-Time	TON = open, TON = V_{CC} (Note 2)				500	ns
	TON = GND, TON = REF (Note 2)				375	
Quiescent Supply Current (V_{CC})	Measured at V_{CC}, with FBS, OUT2, FB2, and LINFB forced above the no-load regulation point				4500	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = -40°C to +100°C**, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Partial Shutdown Supply Current (Linear Regulator On Only)	$V_{SKP1/\overline{SDN}}$ = 0V, $V_{SKP2/\overline{SDN}}$ = 0V, $V_{LIN/\overline{SDN}}$ = 5V; measured at V_{CC}, with FBS and LINFB forced above the no-load regulation point				750	µA
Partial Shutdown Supply Current (BUCK1 and Linear Regulator)	$V_{SKP1/\overline{SDN}}$ = 5V, $V_{SKP2/\overline{SDN}}$ = 0V, $V_{LIN/\overline{SDN}}$ = 5V; measured at V_{CC}, with FBS and LINFB forced above the no-load regulation point				3400	µA
Partial Shutdown Supply Current (BUCK2 Only)	$V_{SKP1/\overline{SDN}}$ = 0V, $V_{SKP2/\overline{SDN}}$ = 5V, $V_{LIN/\overline{SDN}}$ = 0V; measured at V_{CC}, with OUT2 and FB2 forced above the regulation point				1400	µA
Quiescent Supply Current (V_{DD})	Measured at V_{DD}, with FBS, OUT2, and FB2 forced above the no-load regulation point, T_A = -40°C to +85°C				5	µA
Quiescent Battery Current	Measured at V+				40	µA
Shutdown Supply Current (V_{CC})	$V_{SKP1/\overline{SDN}}$ = 0V, $V_{SKP2/\overline{SDN}}$ = 0V, and $V_{LIN/\overline{SDN}}$ = 0V, T_A = -40°C to +85°C				10	µA
Shutdown Supply Current (V_{DD})	$V_{SKP1/\overline{SDN}}$ = 0V, $V_{SKP2/\overline{SDN}}$ = 0V, and $V_{LIN/\overline{SDN}}$ = 0V, T_A = -40°C to +85°C				5	µA
Shutdown Battery Current	$V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = 0V, measured at V+, with V_{CC} = V_{DD} = 0V or 5V, T_A = -40°C to +85°C				5	µA
Reference Voltage	V_{CC} = 4.5V to 5.5V, I_{REF} = 50µA sourcing		1.98		2.02	V
Reference Load Regulation	I_{REF} = 0 to 50µA		0		7	mV
	I_{REF} = 50µA to 100µA		0		7	
Reference Sink Current	REF in regulation		10			µA
OVPSET Disable Mode Threshold	Voltage at OVPSET above which the OVP functions are disabled for BUCK1 and BUCK2		V_{CC} - 1.5		V_{CC} - 0.5	V
OVPSET Default Mode Threshold for BUCK1	Voltage at OVPSET below which the OVP thresholds are set to their default values		0.4		0.6	V
Overvoltage Trip Threshold for BUCK1 (Fixed OVP Threshold)	OVPSET = GND, measured at FBS	MAX1816	1.95		2.05	V
		MAX1994	2.20		2.30	
Overvoltage Trip Threshold for BUCK1 (Adjustable Threshold)	V_{OVPSET} = 1.0V, measured at FBS	MAX1816	0.95		1.05	V
		MAX1994	1.075		1.175	
	V_{OVPSET} = 2.0V, measured at FBS	MAX1816	1.95		2.05	
		MAX1994	2.20		2.30	
Overvoltage Trip Threshold for BUCK2	Measured at OUT2 (or FB2 if external feedback is used)		113		117	%
Output Undervoltage Protection Threshold	With respect to unloaded output voltage FBS and OUT2 (FB2 in external feedback)		65		75	%

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = -40°C to +100°C**, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ILIM1 Default Threshold		V_{CC} - 1.5		V_{CC} - 0.5	V
BUCK1 Current-Limit Threshold (Fixed)	CS1+ - CS1-; V_{ILIM1} = V_{CC}	40		60	mV
BUCK1 Current-Limit Threshold (Adjustable)	CS1+ - CS1-; V_{ILIM1} = 0.5V	40		60	mV
	CS1+ - CS1-; V_{ILIM1} = 2.0V	160		240	
BUCK1 Negative Current-Limit Threshold (Fixed)	CS1+ - CS1-; V_{ILIM1} = V_{CC}	-90		-55	mV
ILIM2 Default Threshold		V_{CC} - 1.5		V_{CC} - 0.5	V
BUCK2 Current-Limit Threshold (Fixed)	AGND - CS2; V_{ILIM2} = V_{CC}	40		60	mV
BUCK2 Current-Limit Threshold (Adjustable)	AGND - CS2; V_{ILIM2} = 0.5V	40		60	mV
	AGND - CS2; V_{ILIM2} = 2.0V	160		240	
BUCK2 Negative Current-Limit Threshold (Fixed)	AGND - CS2; V_{ILIM2} = V_{CC}	-90		-55	mV
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV	4.10		4.45	V
DH1 Gate-Driver On-Resistance	BST1–LX1 forced to 5V (Note 4)			4.5	Ω
DL1 Gate-Driver On-Resistance	DL1 high state (pullup) (Note 4)			4.5	Ω
	DL1 low state (pulldown) (Note 4)			2	
DH2 Gate-Driver On-Resistance	BST2–LX1 forced to 5V (Note 4)			8	Ω
DL2 Gate-Driver On-Resistance	DL2 high state (pullup) (Note 4)			8	Ω
	DL2 low state (pulldown) (Note 4)			3	
LINBSE Drive Current	V_{LINFB} = 1.05V, V_{LINBSE} = 5V			0.4	mA
	V_{LINFB} = 0.965V, V_{LINBSE} = 0.5V	20			
LINFB Regulation Voltage	V_{LINBSE} = 5V, I_{LINBSE} = 4mA (sink)	0.988		1.017	V
LINFB Load Regulation	V_{LINBSE} = 5V, I_{LINBSE} = 2mA to 10mA (sink)	-2.2			%
Logic Input High Voltage	D0–D4, SUS, PERF, LIN/$\overline{SDN}$	2.4			V
Logic Input Low Voltage	D0–D4, SUS, PERF, LIN/$\overline{SDN}$			0.8	V
Logic Input High Voltage	$\overline{DPSLP}$	0.8			V
Logic Input Low Voltage	$\overline{DPSLP}$			0.4	V
Four-Level Logic V_{CC} Level	TON, S0, S1, GAIN logic input high level	V_{CC} - 0.4			V
Four-Level Logic Float Level	TON, S0, S1, GAIN logic input upper midlevel	3.15		3.85	V
Four-Level Logic REF Level	TON, S0, S1, GAIN logic input lower midlevel	1.65		2.35	V
Four-Level Logic GND Level	TON, S0, S1, GAIN logic input low level			0.5	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{OUT1} = 1.20V, V_{OUT2} = 2.50V, V_{CC} = V_{DD} = 5.0V, $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5.0V, **T_A = -40°C to +100°C**, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ Skip Level	SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ logic input high level	2.8			V
SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ PWM Level	SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ logic input float level	1.4		2.2	V
SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ Shutdown Level	SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$ logic input low level			0.4	V
PGOOD Lower Trip Threshold	Measured at FBS, OUT2, and FB2 with respect to unloaded output voltage, falling edge, typical hysteresis = 1%	-12.5		-7.5	%
LINGOOD Lower Trip Threshold and LINFB Undervoltage Protection Threshold	Measured at LINFB with respect to unloaded output voltage, falling edge (Note 5)	-12.5		-7.5	%
PGOOD Upper Trip Threshold	Measured at FBS, OUT_, FB2 with respect to unloaded output voltage, rising edge, typical hysteresis = 1%	7.5		12.5	%
LINGOOD Upper Trip Threshold and LINFB Overvoltage Trip Threshold	Measured at LINFB with respect to unloaded output voltage, rising edge (Note 5)	7.5		12.5	%
LINGOOD Turn-On Delay	LINFB forced 2% above LINGOOD lower trip threshold	1			ms
Open-Drain Output Low Voltage (PGOOD, LINGOOD)	I_{SINK} = 3mA			0.4	V
OFS Positive Offset when Programmed to Zero	Deviation in the output voltage when tested with OFS_ connected to REF			2	mV
OFS Gain	ΔV_{OUT} / ΔV_{OFS}, ΔV_{OFS} = (0.8V - 0V)	0.119		0.131	V/V
	ΔV_{OUT} / ΔV_{OFS}, ΔV_{OFS} = (2.0V - 1.2V)	0.119		0.131	

Note 1: DC output accuracy specifications for BUCK2 refer to the trip level of the error amp. The output voltage has a DC regulation higher than the trip level by 50% of the ripple. In SKIP mode, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

Note 2: On-time and minimum off-time specifications for both BUCK1 and BUCK2 are measured from 50% to 50% at the DH_ pin with LX_ forced to zero, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times can be different due to MOSFET switching speeds.

Note 3: This does not include the time for REF to start up if required.

Note 4: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the thin QFN package.

Note 5: The LINGOOD signal is latched low under a fault condition of LINFB dropping below 90% or rising above 110% of the nominal set point. The LINGOOD signal does not go high again until the fault latch is reset.

Note 6: Specifications from -40°C to +100°C are guaranteed by design, not production tested.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

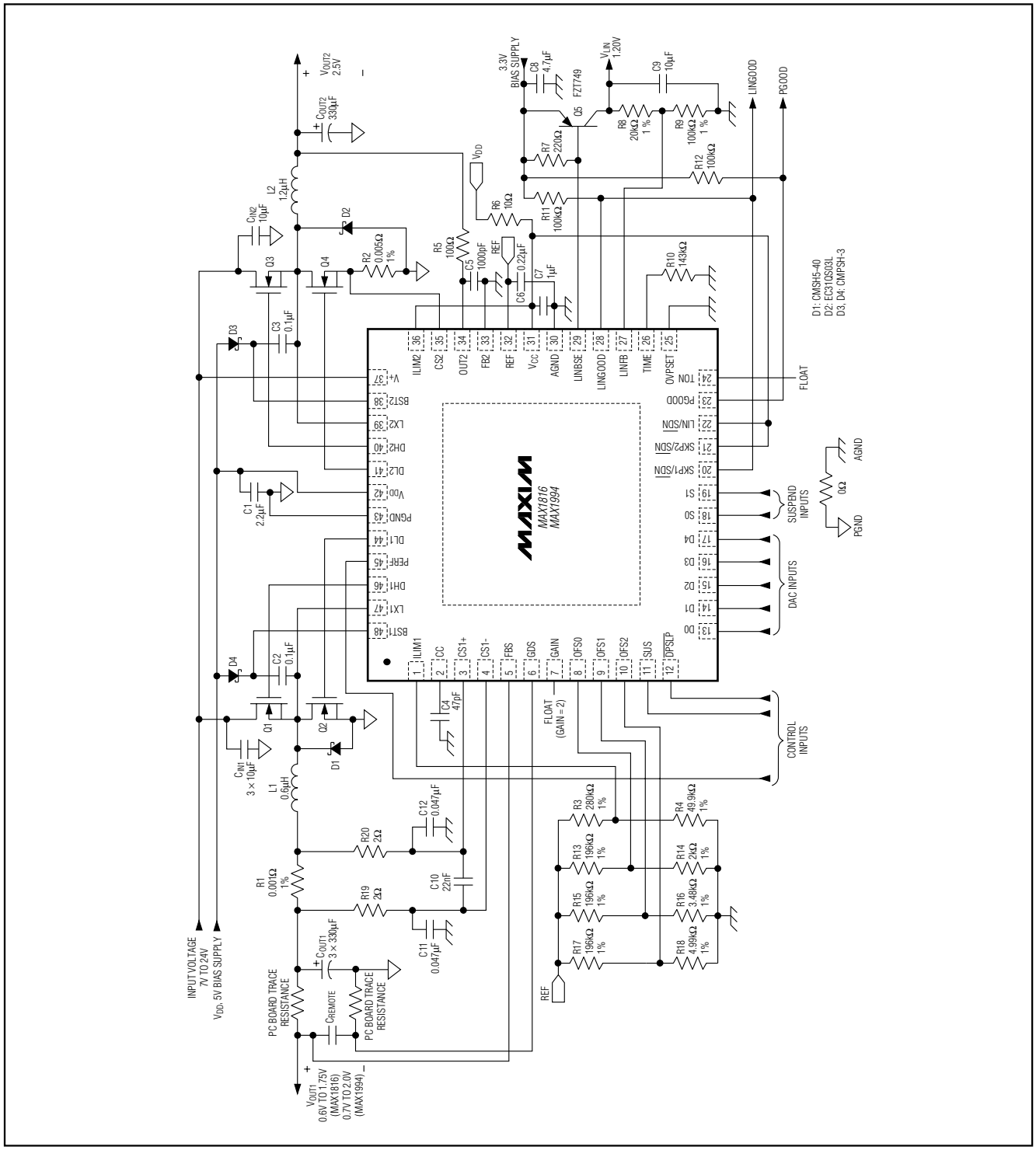


Figure 1. Standard Application Circuit

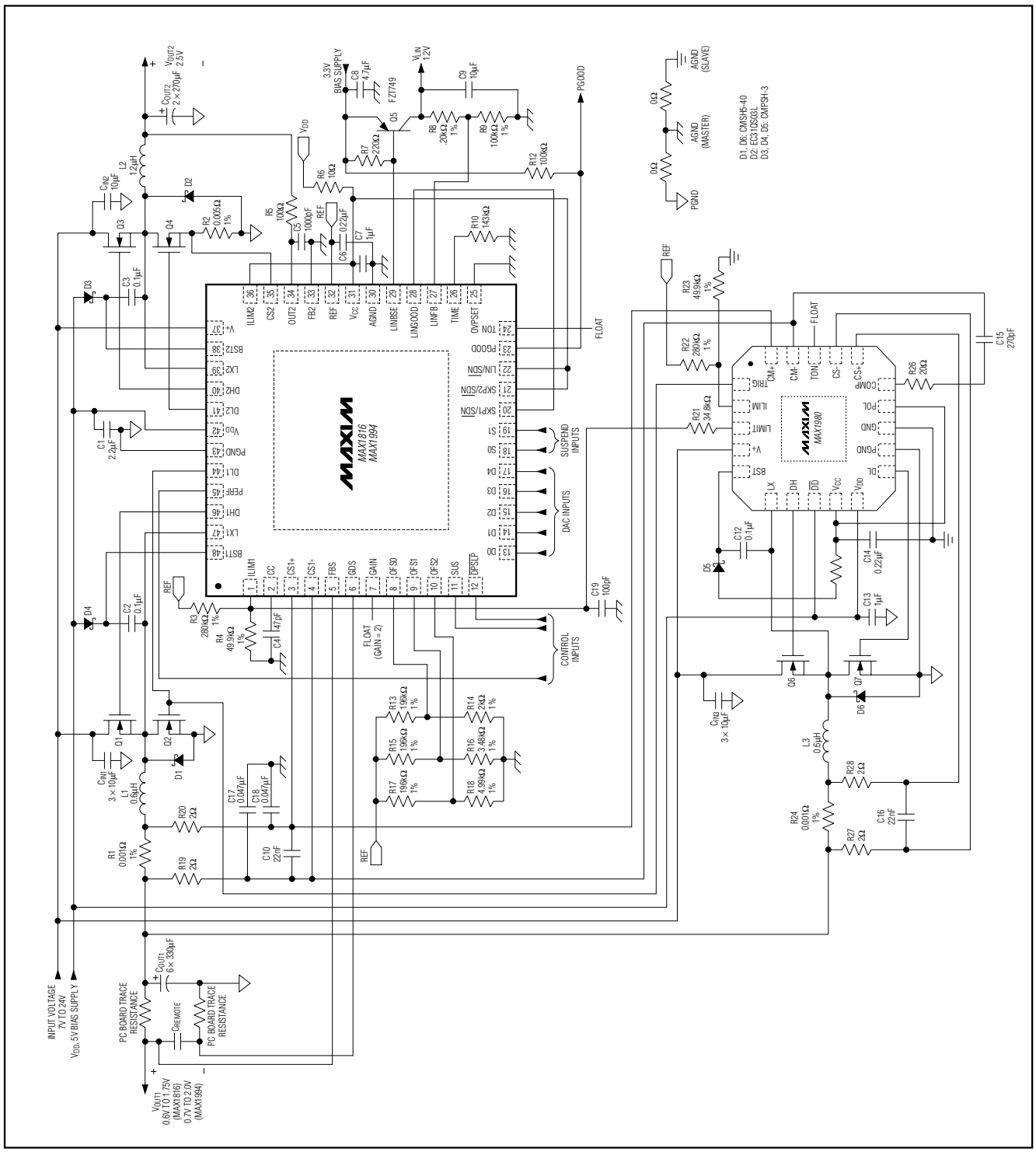


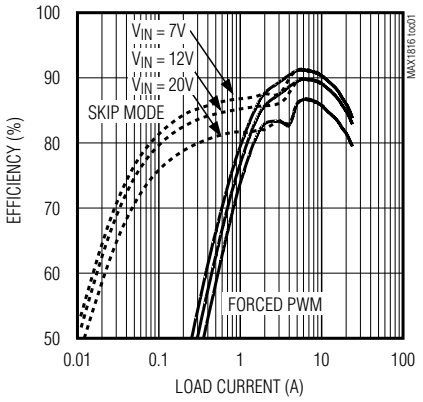
Figure 2. High-Current Master-Slave Application Circuit

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

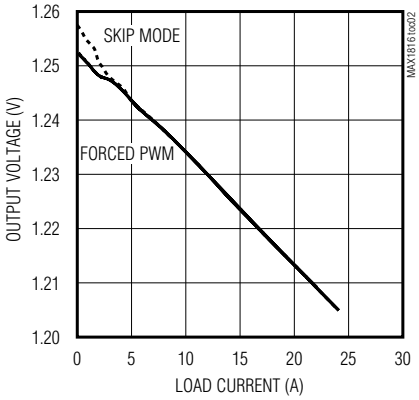
Typical Operating Characteristics

(Circuit of Figure 1, V+ = 12V, V_{DD} = V_{CC} = $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5V; $V_{IN(LDO)}$ = 3.3V, $V_{OUT(BUCK1)}$ = 1.25V, $V_{OUT(BUCK2)}$ = 2.5V; T_A = +25°C, unless otherwise noted.)

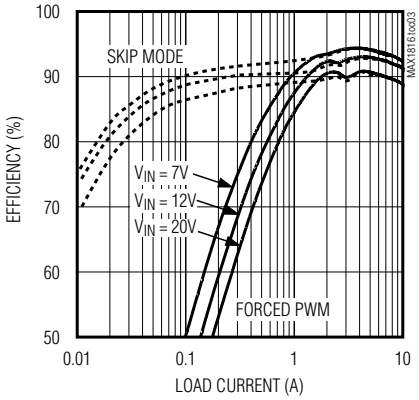
EFFICIENCY vs. LOAD CURRENT (BUCK1 V_{OUT1} = 1.25V)



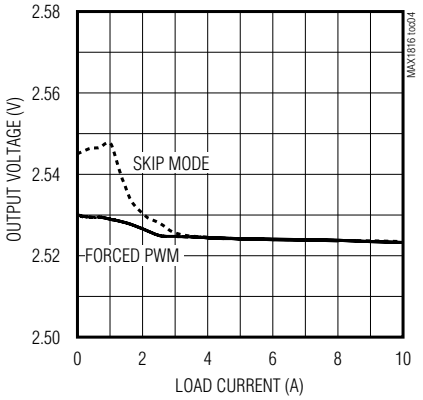
OUTPUT VOLTAGE vs. LOAD CURRENT (BUCK1)



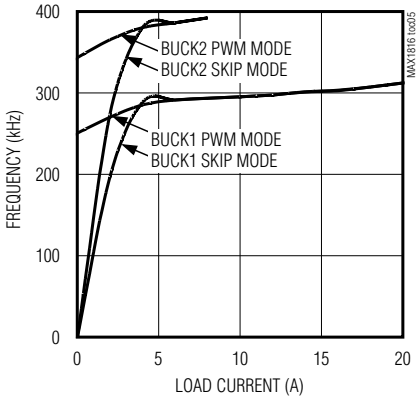
EFFICIENCY vs. LOAD CURRENT (BUCK2 V_{OUT2} = 2.5V)



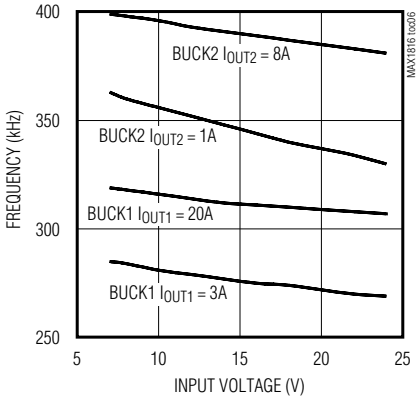
OUTPUT VOLTAGE vs. LOAD CURRENT (BUCK2)



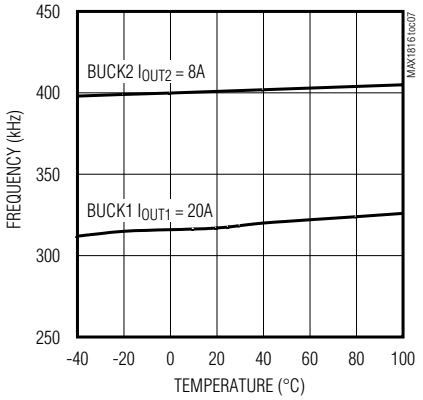
FREQUENCY vs. LOAD CURRENT (BUCK1 AND BUCK2)



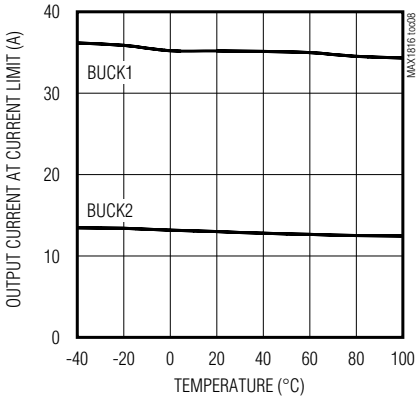
FREQUENCY vs. INPUT VOLTAGE (BUCK1 AND BUCK2)



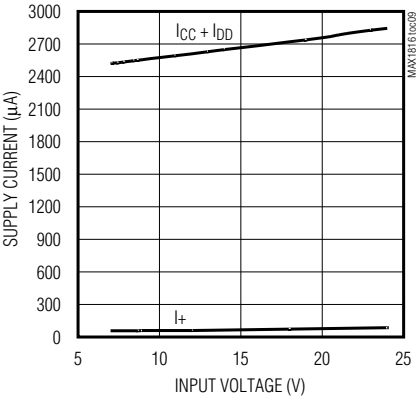
FREQUENCY vs. TEMPERATURE (BUCK1 AND BUCK2)



OUTPUT CURRENT AT CURRENT LIMIT vs. TEMPERATURE



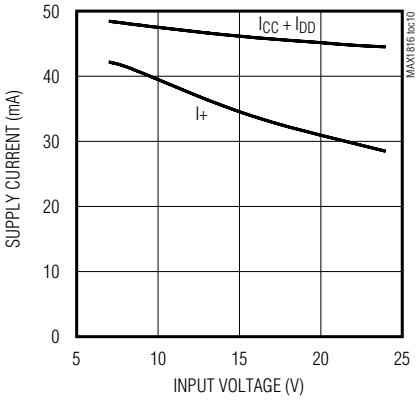
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP MODE)



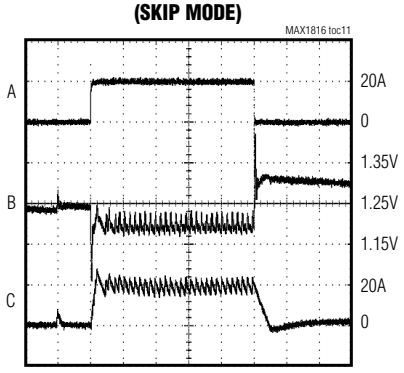
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V+ = 12V, V_{DD} = V_{CC} = $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5V; $V_{IN(LDO)}$ = 3.3V, $V_{OUT(BUCK1)}$ = 1.25V, $V_{OUT(BUCK2)}$ = 2.5V; T_A = +25°C, unless otherwise noted.)

NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (PWM MODE)

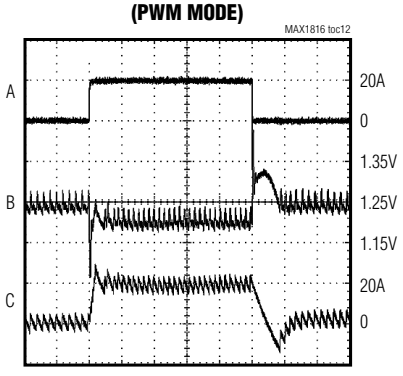


BUCK1 LOAD TRANSIENT RESPONSE (SKIP MODE)



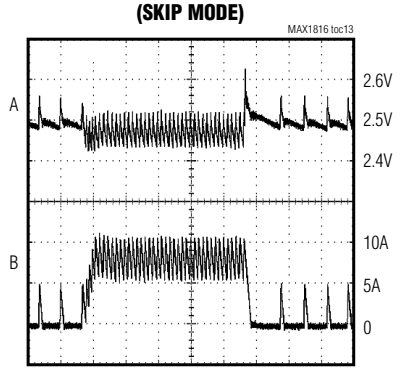
A: LOAD CURRENT, 20A/div
B: OUTPUT VOLTAGE, 100mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 20A/div

BUCK1 LOAD TRANSIENT RESPONSE (PWM MODE)



A: LOAD CURRENT, 20A/div
B: OUTPUT VOLTAGE, 100mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 20A/div

BUCK2 LOAD TRANSIENT RESPONSE (SKIP MODE)



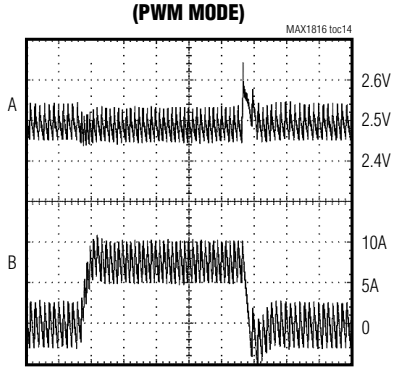
A: OUTPUT VOLTAGE, 100mV/div, AC-COUPLED
B: INDUCTOR CURRENT, 5A/div

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Typical Operating Characteristics (continued)

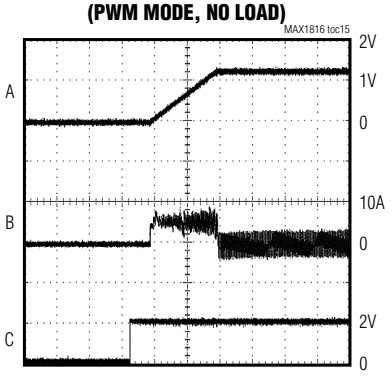
(Circuit of Figure 1, V+ = 12V, V_{DD} = V_{CC} = $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5V; $V_{IN(LDO)}$ = 3.3V, $V_{OUT(BUCK1)}$ = 1.25V, $V_{OUT(BUCK2)}$ = 2.5V; T_A = +25°C, unless otherwise noted.)

BUCK2 LOAD TRANSIENT RESPONSE (PWM MODE)



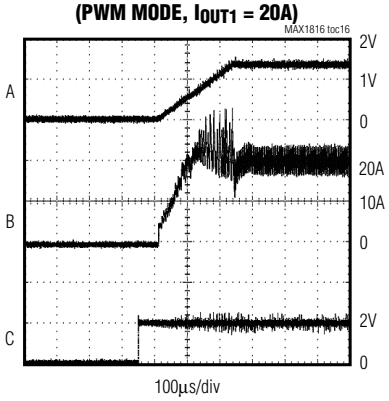
A: OUTPUT VOLTAGE, 100mV/div, AC-COUPLED
B: INDUCTOR CURRENT, 5A/div

BUCK1 STARTUP WAVEFORM (PWM MODE, NO LOAD)



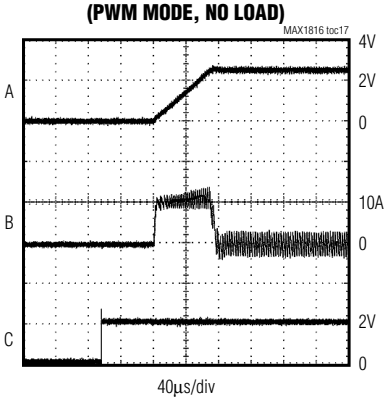
A: OUTPUT VOLTAGE, 1V/div
B: INDUCTOR CURRENT, 10A/div
C: SKP1/SDN SIGNAL, 2V/div

BUCK1 STARTUP WAVEFORM (PWM MODE, I_{OUT1} = 20A)



A: OUTPUT VOLTAGE, 1V/div
B: INDUCTOR CURRENT, 10A/div
C: SKP1/SDN SIGNAL, 2V/div

BUCK2 STARTUP WAVEFORM (PWM MODE, NO LOAD)

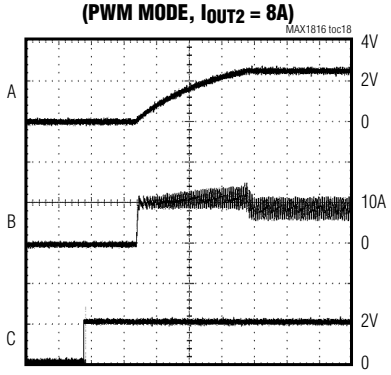


A: OUTPUT VOLTAGE, 2V/div
B: INDUCTOR CURRENT, 10A/div
C: SKP2/SDN SIGNAL, 2V/div

Typical Operating Characteristics (continued)

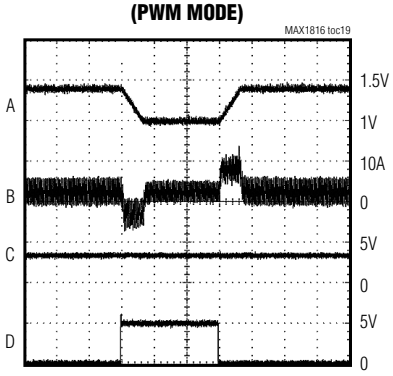
(Circuit of Figure 1, V+ = 12V, V_{DD} = V_{CC} = $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5V; $V_{IN(LDO)}$ = 3.3V, $V_{OUT(BUCK1)}$ = 1.25V, $V_{OUT(BUCK2)}$ = 2.5V; T_A = +25°C, unless otherwise noted.)

BUCK2 STARTUP WAVEFORM (PWM MODE, I_{OUT2} = 8A)



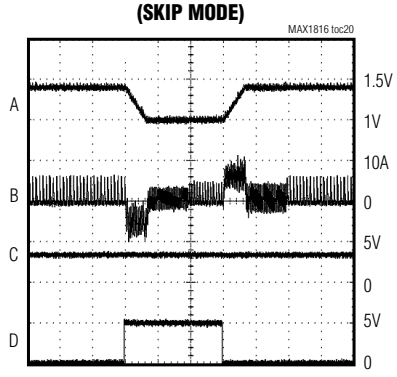
40µs/div
A: OUTPUT VOLTAGE, 2V/div
B: INDUCTOR CURVE CURRENT, 10A/div
C: SKP2/SDN SIGNAL, 2V/div

BUCK1 DYNAMIC OUTPUT-VOLTAGE TRANSITION (PWM MODE)



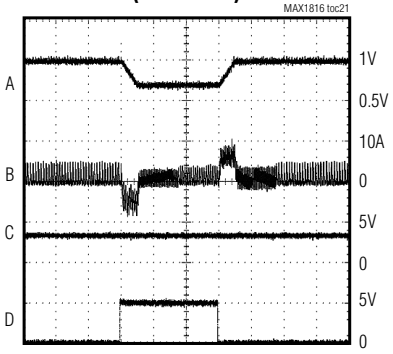
100µs/div
V_{OUT1} = 1.40V TO 1.00V TO 1.40V
I_{OUT1} = 3A, R_{TIME} = 143kΩ
A: OUTPUT VOLTAGE, 500mV/div
B: INDUCTOR CURRENT, 10A/div
C: PGOOD SIGNAL, 5V/div
D: VID BIT, 5V/div

BUCK1 DYNAMIC OUTPUT-VOLTAGE TRANSITION (SKIP MODE)



100µs/div
V_{OUT1} = 1.40V TO 1.00V TO 1.40V
I_{OUT1} = 1A, R_{TIME} = 143kΩ
A: OUTPUT VOLTAGE, 500mV/div
B: INDUCTOR CURRENT, 10A/div
C: PGOOD SIGNAL, 5V/div
D: VID BIT, 5V/div

BUCK1 DYNAMIC OUTPUT-VOLTAGE TRANSITION (SKIP MODE)



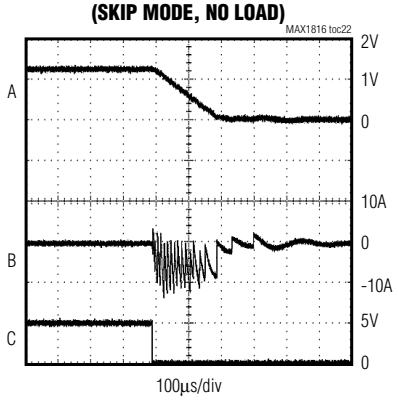
100µs/div
V_{OUT1} = 1.00V TO 0.60V TO 1.00V
I_{OUT1} = 1A, R_{TIME} = 143kΩ
A: OUTPUT VOLTAGE, 500mV/div
B: INDUCTOR CURRENT, 10A/div
C: PGOOD SIGNAL, 5V/div
D: SUS SIGNAL, 5V/div

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Typical Operating Characteristics (continued)

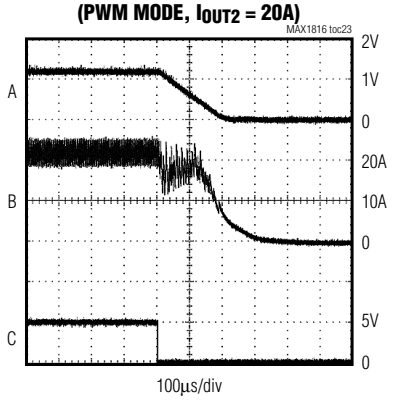
(Circuit of Figure 1, V+ = 12V, V_{DD} = V_{CC} = $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5V; $V_{IN(LDO)}$ = 3.3V, $V_{OUT(BUCK1)}$ = 1.25V, $V_{OUT(BUCK2)}$ = 2.5V; T_A = +25°C, unless otherwise noted.)

BUCK1 SHUTDOWN WAVEFORM (SKIP MODE, NO LOAD)



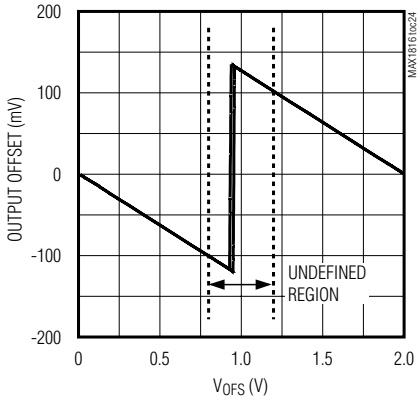
A: OUTPUT VOLTAGE, 1V/div
B: INDUCTOR CURRENT, 10A/div
C: SKP1/SDN SIGNAL, 5V/div

BUCK1 SHUTDOWN WAVEFORM (PWM MODE, I_{OUT2} = 20A)

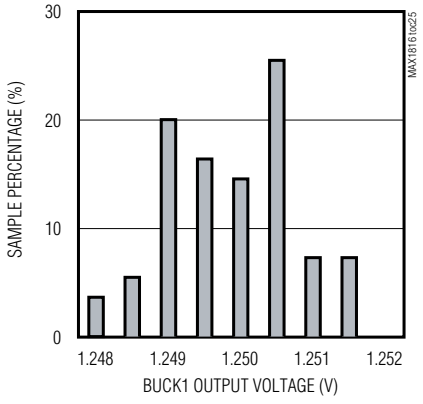


A: OUTPUT VOLTAGE, 1V/div
B: INDUCTOR CURRENT, 10A/div
C: SKP1/SDN SIGNAL, 5V/div

OUTPUT OFFSET vs. OFS INPUT VOLTAGE



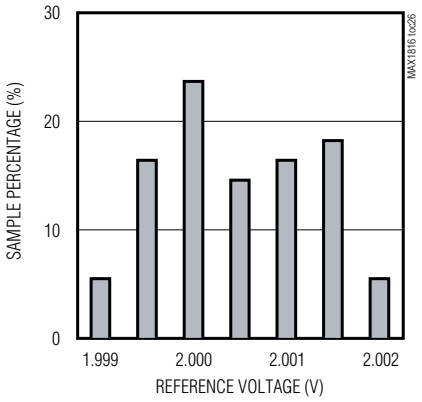
BUCK1 OUTPUT-VOLTAGE DISTRIBUTION (V_{OUT1} = 1.25V, SAMPLE SIZE = 55)



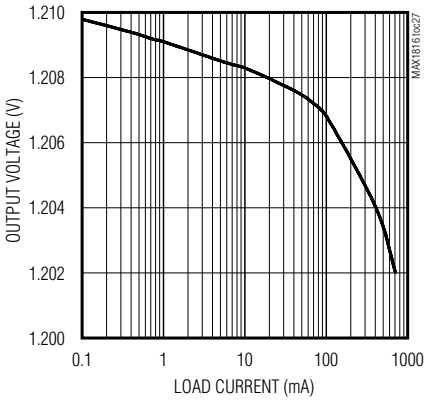
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V+ = 12V, V_{DD} = V_{CC} = $V_{SKP1/\overline{SDN}}$ = $V_{SKP2/\overline{SDN}}$ = $V_{LIN/\overline{SDN}}$ = 5V; $V_{IN(LDO)}$ = 3.3V, $V_{OUT(BUCK1)}$ = 1.25V, $V_{OUT(BUCK2)}$ = 2.5V; T_A = +25°C, unless otherwise noted.)

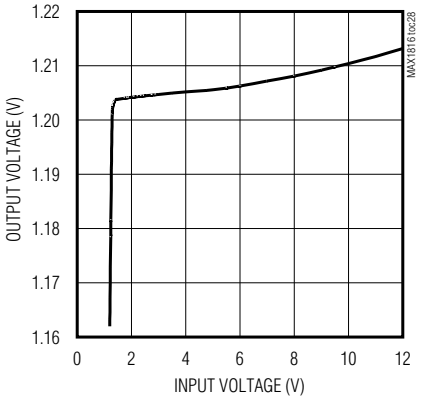
REFERENCE VOLTAGE DISTRIBUTION
(V_{REF} = 2.0V, SAMPLE SIZE = 55)



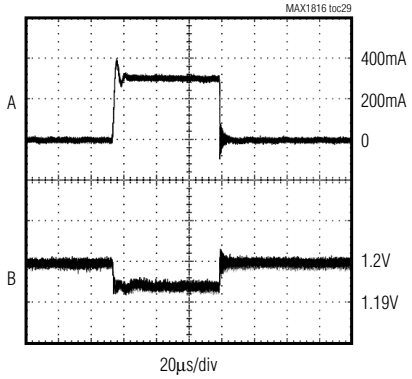
LINEAR REGULATOR LOAD REGULATION



LINEAR REGULATOR LINE REGULATION

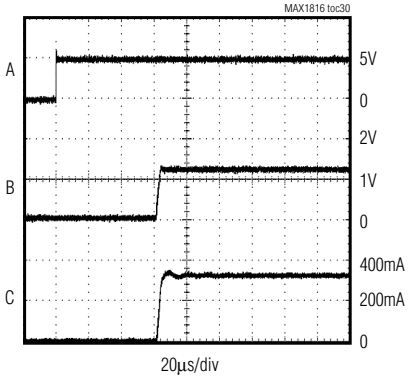


LINEAR REGULATOR LOAD TRANSIENT RESPONSE



A: LOAD CURRENT, 200mA/div
B: OUTPUT VOLTAGE, 10mV/div, AC-COUPLED

LINEAR REGULATOR STARTUP WAVEFORM



A: $V_{LIN/\overline{SDN}}$, 5V/div
B: V_{LIN} = 1.2V, 1V/div
C: I_{LIN} = 300mA, 200mA/div

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Pin Description

PIN	NAME	FUNCTION
1	ILIM1	BUCK1 Current-Limit Adjustment. The CS1+ - CS1- current-limit threshold defaults to 50mV if ILIM1 is connected to V_{CC}. In adjustable mode, the current-limit threshold voltage is precisely 1/10th of the voltage at ILIM1. The logic threshold for switchover to the default value is approximately V_{CC} - 1V.
2	CC	Integrator Time Constant Control Input. This pin allows the integrator to be compensated independent of the voltage-positioning sense feedback path. Connect a 47pF to 1000pF capacitor from this pin to ground to control the integration time constant.
3	CS1+	Positive Voltage-Positioning and Current-Sense Input for BUCK1. The current-limit sense voltage for CS1+ - CS1- is 1/10th of the voltage at the ILIM1 input. The CS1+ and CS1- inputs are also used for active voltage positioning, with the voltage-positioning gain set with the GAIN pin. Connecting the GAIN pin to ground disables voltage positioning. Positive and negative current limits are always active.
4	CS1-	Negative Voltage-Positioning and Current-Sense Input for BUCK1. CS1- is also the output sense input for calculating TON. The current-limit sense voltage for CS1+ - CS1- is 1/10th of the voltage at the ILIM1 input. The CS1+ and CS1- inputs are also used for active voltage positioning, with the voltage-positioning gain set with the GAIN pin. Connecting the GAIN pin to ground disables voltage positioning. Positive and negative current limits are always active.
5	FBS	Output Feedback Remote-Sense Input for BUCK1. Connect FBS directly to the load. FBS internally connects to an amplifier that fine-tunes the output voltage, compensating for voltage drops from the regulator output to the load.
6	GDS	Ground Remote-Sense Input for BUCK1. Connect GDS directly to the load. GDS internally connects to an amplifier that fine-tunes the output voltage, compensating for voltage drops from the regulator ground to the load ground.
7	GAIN	Voltage-Positioning Gain Control. GAIN is a four-level logic input that selects the voltage-positioning gain (see *CS1+, CS1-* pins). The gain setting does not affect current-limit functions. Connecting GAIN to GND disables the voltage positioning by setting the gain to zero. Connecting GAIN to REF sets the gain to 1.5. Leaving GAIN open sets the gain to 2. Connecting GAIN to V_{CC} sets the gain to 4. GND = 0; REF = 1.5; open = 2; V_{CC} = 4.
8	OFS0	Voltage-Divider Input for Voltage-Positioning Offset Control. OFS0–OFS2 are selected based on the SUS, PERF, and $\overline{DPSLP}$ signals. For 0V < OFS_ < 0.8V, 0.125 times the voltage at OFS_ is subtracted from the output. For 1.2V < OFS_ < 2.0V, 0.125 times the difference between REF and OFS_ is added to the output. Voltages in the range of 0.8V < OFS_ < 1.2V are not permitted (see Table 7).
9	OFS1	Voltage-Divider Input for Voltage-Positioning Offset Control. OFS0–OFS2 are selected based on the SUS, PERF, and $\overline{DPSLP}$ signals. For 0V < OFS_ < 0.8V, 0.125 times the voltage at OFS_ is subtracted from the output. For 1.2V < OFS_ < 2.0V, 0.125 times the difference between REF and OFS_ is added to the output. Voltages in the range of 0.8V < OFS_ < 1.2V are not permitted (see Table 7).
10	OFS2	Voltage-Divider Input for Voltage-Positioning Offset Control. OFS0–OFS2 are selected based on the SUS, PERF, and $\overline{DPSLP}$ signals. For 0V < OFS_ < 0.8V, 0.125 times the voltage at OFS_ is subtracted from the output. For 1.2V < OFS_ < 2.0V, 0.125 times the difference between REF and OFS_ is added to the output. Voltages in the range of 0.8V < OFS_ < 1.2V are not permitted (see Table 7).
11	SUS	Suspend Mode Control Input. The SUS signal causes the S0 and S1 inputs to take precedence over the VID code setting and OFS inputs. When SUS is high, the state of the S0 and S1 inputs are decoded to select the appropriate DAC code and the offset is forced to zero (see the *DAC Inputs and Internal Multiplexer* section).
12	$\overline{DPSLP}$	Deep Sleep Control Input. This logic control input goes to the offset selection multiplexer that determines which, if any, offset control inputs are read (OFS0–OFS2). This input is compatible with 1.5V logic (see Table 7).
13	D0	VID Code Input. D0 is the least significant bit (LSB).

Pin Description (continued)

PIN	NAME	FUNCTION
14	D1	VID Code Input
15	D2	VID Code Input
16	D3	VID Code Input
17	D4	VID Code Input. D4 is the most significant bit (MSB).
18	S0	Suspend Mode Voltage-Select Input. S0 and S1 are four-level logic inputs that select the suspend mode VID code for the suspend mode multiplexer inputs. If SUS is high, the suspend mode VID code is delivered to the DAC overriding any other voltage setting (see the *DAC Inputs and Internal Multiplexer* section).
19	S1	Suspend Mode Voltage-Select Input. S0 and S1 are four-level logic inputs that select the suspend mode VID code for the suspend mode multiplexer inputs. If SUS is high, the suspend mode VID code is delivered to the DAC overriding any other voltage setting (see the *DAC Inputs and Internal Multiplexer* section).
20	SKP1/$\overline{SDN}$	Combined Shutdown and Skip-Mode Control Input for BUCK1. Always start BUCK2 before starting BUCK1. Connect SKP1/$\overline{SDN}$ to V_{CC} or drive the pin above 2.8V with external 3.3V-powered CMOS logic for normal PFM/PWM operation. Connect SKP1/$\overline{SDN}$ to GND or drive the pin below 0.5V to shut down BUCK1. In shutdown mode, DL1 is forced to V_{DD} in order to enforce overvoltage protection when the regulator is powered down. Leave SKP1/$\overline{SDN}$ floating for the low-noise forced PWM operation. Low-noise forced-PWM mode causes the inductor current to reverse at light loads and suppresses pulse-skipping operation. SKP1/$\overline{SDN}$ can also be used to disable both over- and undervoltage protection circuits and clear the fault latch. This test mode is enabled by forcing the pin to 10.8V < $V_{SKP1/\overline{SDN}}$ < 13.2V. While in the test mode, the regulator performs the normal PFM/PWM operation. SKP1/$\overline{SDN}$ cannot withstand the battery voltage.
21	SKP2/$\overline{SDN}$	Combined Shutdown and Skip-Mode Control Input for BUCK2. Always start BUCK2 before starting BUCK1. Connect SKP2/$\overline{SDN}$ to V_{CC} or drive the pin above 2.8V with external 3.3V-powered CMOS logic for normal PFM/PWM operation. Connect SKP2/$\overline{SDN}$ to GND or drive the pin below 0.5V to shut down BUCK2. In shutdown mode, DL2 is forced to V_{DD} if the overvoltage protection is enabled. This is done in order to enforce overvoltage protection even when the regulator is powered down. Leave SKP2/$\overline{SDN}$ floating for the low-noise forced PWM operation. Low-noise forced-PWM mode causes the inductor current to recirculate at light loads and suppresses pulse-skipping operation. If OVPSET = V_{CC}, then DL2 is forced LOW in shutdown mode. SKP2/$\overline{SDN}$ cannot withstand the battery voltage.
22	LIN/$\overline{SDN}$	Linear Regulator Shutdown Control Input. Connect LIN/$\overline{SDN}$ to V_{CC} or drive the pin above 2.4V to turn on the linear regulator. Connect LIN/$\overline{SDN}$ to GND or drive the pin below 0.8V to shut down the linear regulator. In shutdown mode, LINBSE is forced to a high-impedance state preventing sufficient drive to the external PNP power transistor in the regulator. LIN/$\overline{SDN}$ cannot withstand the battery voltage.
23	PGOOD	Open-Drain Power-Good Output. PGOOD is forced low during power-up and power-down transitions on BUCK1. In normal operation, if FBS and OUT2 (FB2) are in regulation, then PGOOD is high. PGOOD is forced low when SKP1/$\overline{SDN}$ is low. If SKP2/$\overline{SDN}$ is low, OUT2 (FB2) does not affect PGOOD. Normally, PGOOD is forced high for all VID transitions, and stays high for 4 TIME clock periods after the D/A count is equalized. If OUT2 is enabled during these conditions and a fault occurs on BUCK2, then PGOOD goes low. A pullup resistor on PGOOD causes additional finite shutdown current.
24	TON	On-Time Selection Control Input. This four-level input sets the K factor that determines the DH on-time. The TON times for BUCK2 are shifted to minimize beating between the two regulators. GND = 1000kHz (BUCK1) and 715kHz (BUCK2), REF = 550kHz (BUCK1) and 390kHz (BUCK2), open = 300kHz (BUCK1) and 390kHz (BUCK2), V_{CC} = 200kHz (BUCK1) and 260kHz (BUCK2).

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Pin Description (continued)

PIN	NAME	FUNCTION
25	OVPSET	Overvoltage Protection Control Input. This pin controls the OVP functions for BUCK1 and BUCK2. LINFB is not affected by OVPSET. Connect OVPSET to V_{CC} to disable overvoltage protection for both BUCK1 and BUCK2. Connect OVPSET to GND for default overvoltage threshold of 2.0V (MAX1816) or 2.25V (MAX1994) for BUCK1, measured at FBS. The OVP threshold for BUCK2 is always at 115% of the nominal output voltage. The OVP threshold for BUCK1 can be adjusted by connecting OVPSET between 1.0V and 2.0V. An overvoltage condition occurs if $V_{FBS} > V_{OVPSET}$ (MAX1816) or $V_{FBS} > 1.125 \times V_{OVPSET}$ (MAX1994). Undervoltage protection thresholds are always enabled and are not affected by this pin.
26	TIME	Slew Rate Adjustment Input. Connect a resistor from TIME to GND to set the internal slew-rate clock. A 680kΩ to 68kΩ resistor to GND sets the clock from 53kHz to 530kHz, $f_{SLEW} = 252kHz \times (143k\Omega / R_{TIME})$.
27	LINFB	Linear Regulator Feedback Input. The linear regulator's feedback set point is 1.0V. Connect a resistive voltage-divider from the collector of the external PNP pass transistor to LINFB. The DC bias current in the voltage-divider should be greater than 10µA. The linear regulator is active whenever LIN/$\overline{SDN}$ is high.
28	LINGOOD	Open-Drain Power-Good Output for the Linear Regulator. As soon as LINFB is in regulation, LINGOOD goes high after a 1ms minimum delay. When the output goes out of regulation or LIN/$\overline{SDN}$ goes low, LINGOOD is forced low within approximately 10µs. A pullup resistor on LINGOOD causes additional shutdown current.
29	LINBSE	Linear Regulator Base Drive. Connect LINBSE to the base of an external PNP power transistor. Add a 220Ω pullup resistor between the base and the emitter.
30	AGND	Analog Ground. Connect the MAX1816/MAX1994s' exposed backside pad and low-current ground terminations to AGND. The current-limit comparator's ground sense for BUCK2 also connects to AGND.
31	V_{CC}	Analog Supply Voltage Input for BUCK1, BUCK2, and the Linear Regulator. This pin supplies all power to the device except for the MOSFET drivers. The range for V_{CC} is 4.5V to 5.5V. Bypass V_{CC} to GND with a minimum capacitance of 1µF. The maximum resistance between V_{CC} and V_{DD} should be 10Ω.
32	REF	2.0V Reference Output. Bypass REF to GND with a minimum capacitance of 0.22µF. The reference is trimmed with a nominal 50µA load, and can source a total of 100µA for external loads. Loading REF greater or less than 50µA decreases output-voltage accuracy according to the limits defined in the *Electrical Characteristics* table.
33	FB2	Adjustable Feedback Input for BUCK2. In adjustable mode, FB2 regulates to 1.00V. It also selects default voltage. Connect FB2 to GND for 2.5V output, or connect FB2 to V_{CC} for 1.8V output.
34	OUT2	Output Voltage Connection for BUCK2. Connect directly to the junction of the output filter capacitors. OUT2 senses the output voltage to determine the on-time and also serve as the feedback input in fixed-output modes.
35	CS2	Current-Sense Input for BUCK2. For accurate current limit, connect CS2 to a sense resistor between the source of the low-side MOSFET and ground. Alternatively, CS2 can be connected to LX2 for lossless current sensing across the low-side MOSFET. The current-limit sense voltage for CS2 is set at the ILIM2
36	ILIM2	BUCK2 Current-Limit Adjustment Input. The current-limit threshold measured between AGND and CS2 defaults to 50mV when ILIM2 is connected to V_{CC}. In adjustable mode, the current-limit threshold voltage is precisely 1/10th of the voltage at ILIM2. The logic threshold for switchover to the default value is approximately V_{CC} - 1V.
37	V+	Battery Voltage Sense Input. V+ is used only for PWM one-shot timing. DH1 and DH2 on-times are inversely proportional to input voltage over a 2V to 28V range.
38	BST2	BUCK2 Boost Flying Capacitor Connection. An optional resistor in series with BST2 allows the DH1 pullup current to be adjusted.

Pin Description (continued)

PIN	NAME	FUNCTION
39	LX2	BUCK2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver.
40	DH2	BUCK2 High-Side Gate-Driver Output. DH2 swings from LX2 to BST2.
41	DL2	BUCK2 Low-Side Gate-Driver Output. DL2 swings from PGND to V_{DD}. DL2 is forced high when MAX1816/MAX1994 detect an overvoltage fault. When the regulator powers down, DL2 is forced high if OVP is enabled, and is forced low if OVP is disabled.
42	V_{DD}	Supply Voltage Input for DL1 and DL2 Gate Drivers. Connect V_{DD} to the system supply voltage (4.5V to 5.5V). Bypass V_{DD} to PGND with a 2.2µF or greater ceramic capacitor.
43	PGND	Power Ground. Ground connection for low-side gate drivers DL1 and DL2.
44	DL1	BUCK1 Low-Side Gate-Driver Output. DL1 swings from PGND to V_{DD}. DL1 is forced high when MAX1816/MAX1994 detect an overvoltage fault. When the regulator powers down, DL1 is forced high.
45	PERF	Performance Mode Control Input. This logic-control input goes to the offset selection mux that determines which, if any, offset control inputs are read (OFS0–OFS2). This input is compatible with 3.3V logic (see Table 7).
46	DH1	BUCK1 High-Side Gate-Driver Output. DH1 swings from LX1 to BST1.
47	LX1	BUCK1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver.
48	BST1	BUCK1 Boost Flying Capacitor Connection. An optional resistor in series with BST1 allows the DH1 pullup current to be adjusted.

Detailed Description

The MAX1816/MAX1994 are dual step-down controllers for notebook computer applications. The controllers include a CPU regulator (BUCK1) that features a dynamically adjustable output with offset control and a programmable suspend mode voltage. This regulator is capable of delivering very large currents at the high efficiencies needed for leading-edge CPU core applications. A second step-down regulator (BUCK2) is included to generate I/O or memory supplies. Both regulators employ Maxim's proprietary Quick-PWM control architecture. A linear-regulator controller is also included for low-voltage auxiliary power supplies. All of the regulators have independent shutdown control inputs. The linear regulator includes a power-good output that is independent of the combined power-good output for BUCK1 and BUCK2.

5V Bias Supply (V_{CC} and V_{DD})

The MAX1816/MAX1994 require an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook computer's 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM controllers and gate drivers of BUCK1 and BUCK2. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator.

The 5V bias supply must provide V_{CC} for the PWM controller's internal reference, bias, and logic; and V_{DD} for the gate drivers. The maximum bias supply current is:

$$I_{BIAS} = I_{CC} + f (Q_{G1} + Q_{G2} + Q_{G3} + Q_{G4})$$
$$= 20mA \text{ to } 80mA \text{ (typ)}$$

where I_{CC} is 2.2mA (typ), f is the switching frequency, and Q_{G1}, Q_{G2}, Q_{G3}, and Q_{G4} are the total gate charge specifications at V_{GS} = 5V in the MOSFET data sheets.

V+ and V_{DD} can be connected if the input power source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the battery supply, the enable signals (SKP_/$\overline{SDN}$) must be delayed until the battery voltage is present to ensure startup.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Table 1. Component Selection for Standard Applications

COMPONENT	BUCK1 (CIRCUITS OF FIGURES 1 AND 2)	BUCK2 (CIRCUITS OF FIGURES 1 AND 2)	SLAVE (CIRCUIT OF FIGURE 2)
Input Voltage Range	7V to 24V	7V to 24V	7V to 24V
Output Voltage	0.6V to 1.75V (MAX1816), 0.7V to 2.0V (MAX1994)	2.5V	0.6V to 1.75V (MAX1816), 0.7V to 2.0V (MAX1994)
Output Current	20A	7A	20A
Frequency	300kHz	300kHz	300kHz
High-Side MOSFET	(2) N-channel International Rectifier IRF7811W	N-channel International Rectifier IRF7811W	(2) N-channel International Rectifier IRF7811W
Low-Side MOSFET	(2) N-channel International Rectifier IRF7822 Fairchild FDS7764A	N-channel International Rectifier IRF7822 Fairchild FDS7764A	(2) N-channel International Rectifier IRF7822 Fairchild FDS7764A
Input Capacitor	(3) 10µF, 25V X5R ceramic Taiyo Yuden TMK432BJ106KM TDK C4532X5R1E106M	10µF, 25V X5R ceramic Taiyo Yuden TMK432BJ106KM TDK C4532X5R1E106M	(3) 10µF, 25V X5R ceramic Taiyo Yuden TMK432BJ106KM TDK C4532X5R1E106M
Output Capacitor	(3) 330µF, 2.5V, 10mΩ SP Panasonic EEFUE0E331XR	(1) 330µF, 2.5V, 10mΩ SP Panasonic EEFUE0E331XR	(3) 330µF, 2.5V, 10mΩ SP Panasonic EEFUE0E331XR
Inductor	0.6µH Panasonic ETQP6F0R6BFA Toko EH125C-R60N Sumida CDEP134H-0R6	1.2µH Toko EH125C-1R2N Sumida CDEP134H-1R2 Panasonic ETQP6F1R2BFA	0.6µH Panasonic ETQP6F0R6BFA Toko EH125C-R60N Sumida CDEP134H-0R6
Current-Sense Resistor	1mΩ ±1%, 1W Panasonic ERJM1WTJ1M0U	5mΩ ±1%, 1W Panasonic ERJM1WSF5M0U	1mΩ ±1%, 1W Panasonic ERJM1WTJ1M0U

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
CAPACITORS		
Panasonic	847-468-5624	www.panasonic.com
Sanyo	619-661-6835	www.sanyovideo.com
Taiyo Yuden	408-573-4150	www.t-yuden.com
TDK	847-803-6100	www. tdk.com
INDUCTORS		
Panasonic	847-468-5624	www.panasonic.com
Sumida	408-982-9660	www.sumida.com
MOSFETs		
Fairchild Semiconductor	888-522-5372	www.fairchildsemi.com
International Rectifier	310-322-3331	www.irf.com
Siliconix	203-268-6261	www.vishay.com

Free-Running, Constant On-Time PWM Controller with Input Feed-Forward

Both BUCK1 and BUCK2 employ Maxim's proprietary Quick-PWM control architecture. The control scheme is a pseudo fixed-frequency, constant-on-time current-mode type with voltage feed forward (Figures 3, 4, and 5). It relies on the output ripple voltage to provide the PWM ramp signal. This signal can come from the output filter capacitor's ESR or a dedicated sense resistor. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (425ns, typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time (Figures 4 and 5). This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltages. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input, and proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output-voltage ripple:

$$\text{On-Time} = K\,(V_{OUT} + 0.075V) / V_{IN}$$

where K is set by the TON pin-strap connection and 0.075V is an approximation to accommodate for the expected drop across the low-side MOSFET switch (Table 3).

The on-times for BUCK1 have nominal frequency settings of 200kHz, 300kHz, 550kHz, or 1000kHz, while the on-times for BUCK2 are shifted to minimize beating between the two regulators. The corresponding frequency settings for BUCK2 are 260kHz, 390kHz, 390kHz, and 715kHz. The BUCK2 on-times for TON = open and TON = V_{CC} are shifted down to improve the efficiency. The BUCK2 on-times for TON = GND and TON = REF are shifted up to avoid beating, yet maintain the efficiency. The latter settings were not shifted down because the resulting frequencies would be too high.

The on-time one-shot has good accuracy at the operating points specified in the *Electrical Characteristics* (±10% at 200kHz and 300kHz, ±12.5% at 550kHz and 1000kHz for BUCK1). On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* can vary over a wider range.

For example, the 1000kHz setting typically runs about 10% slower with inputs much greater than 5V due to the very short on-times required.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* are influenced by switching delays in the external high-side MOSFETs. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PC board copper losses tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in PWM mode (SKP_/$\overline{SDN}$ = open) and during dynamic output-voltage transitions (BUCK1) when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH_ low-to-high dead time.

Table 3. Approximate K-Factor Errors

TON	BUCK1 K-FACTOR (µs)	BUCK1 FREQUENCY (kHz)	BUCK1 K-FACTOR ERROR (%)	BUCK2 K-FACTOR (µs)	BUCK2 FREQUENCY (kHz)	BUCK2 K-FACTOR ERROR (%)
GND	1.0	1000	±12.5	1.4	715	±12.5
Open	1.8	550	±12.5	2.56	390	±10
REF	3.3	300	±10	2.56	390	±10
V_{CC}	5.0	200	±10	3.84	260	±10

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

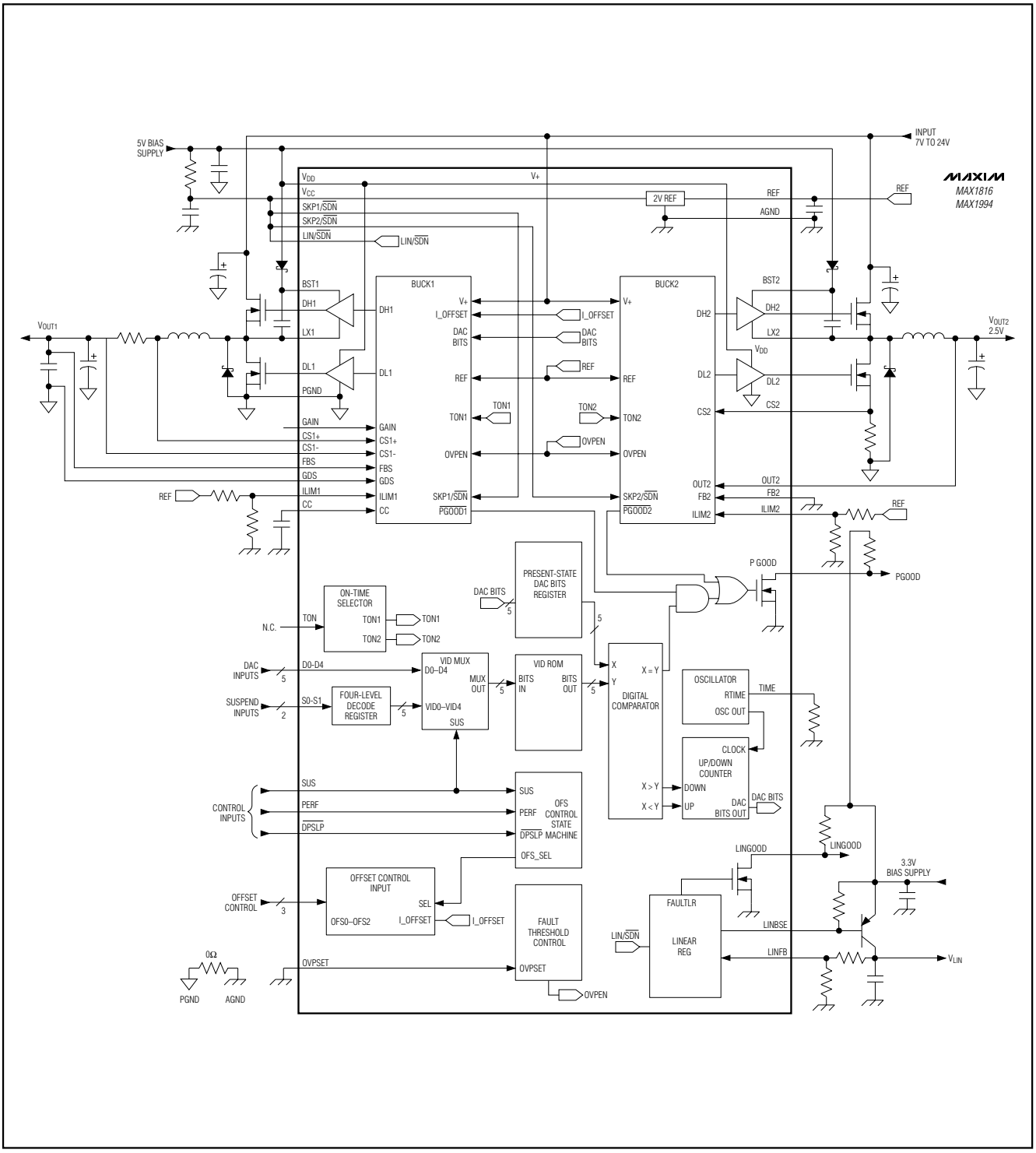


Figure 3. Functional Diagram

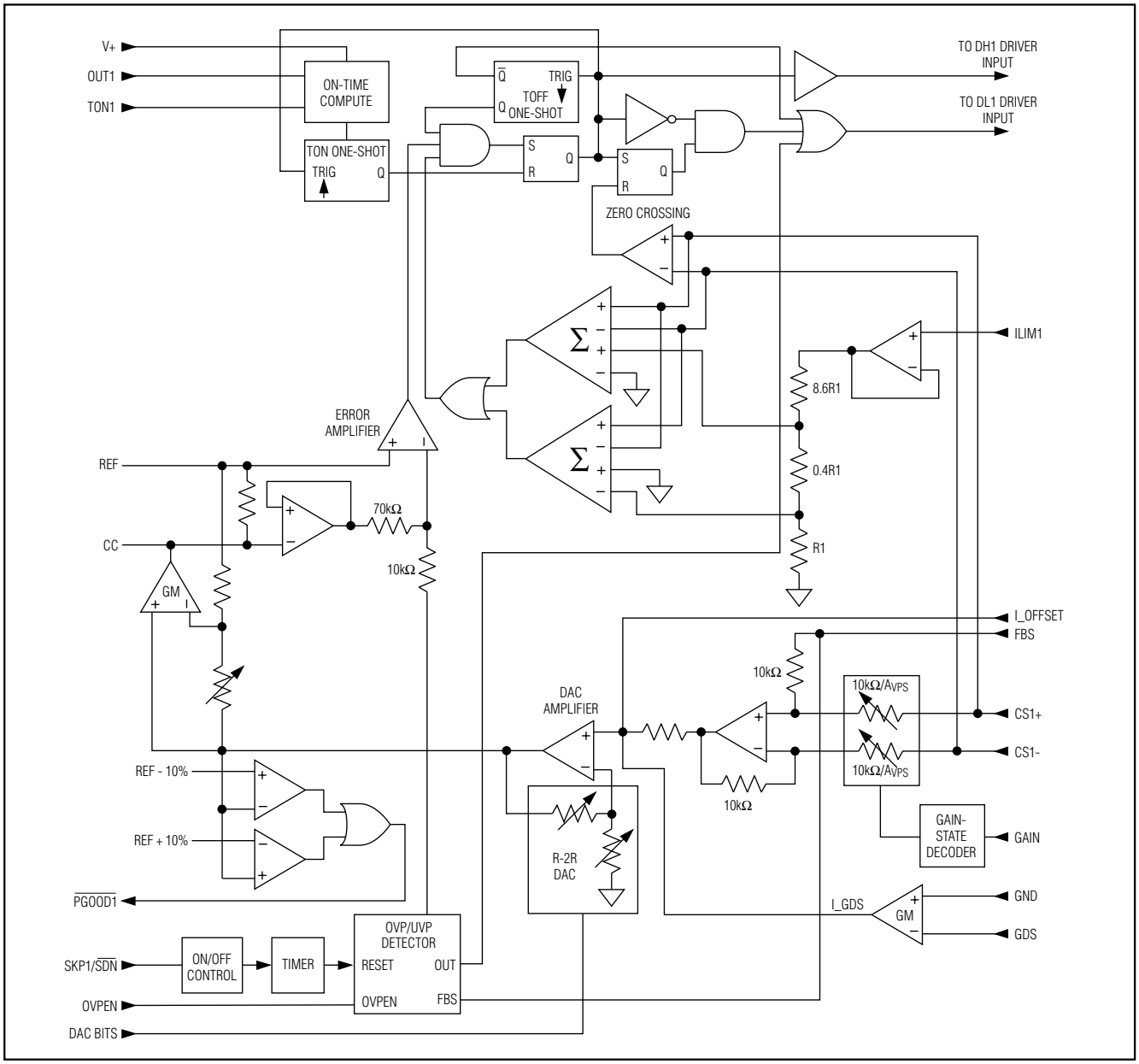


Figure 4. BUCK1 PWM Control Diagram

For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PC board resistances; and t_{ON} is the on-time calculated by the MAX1816/MAX1994.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

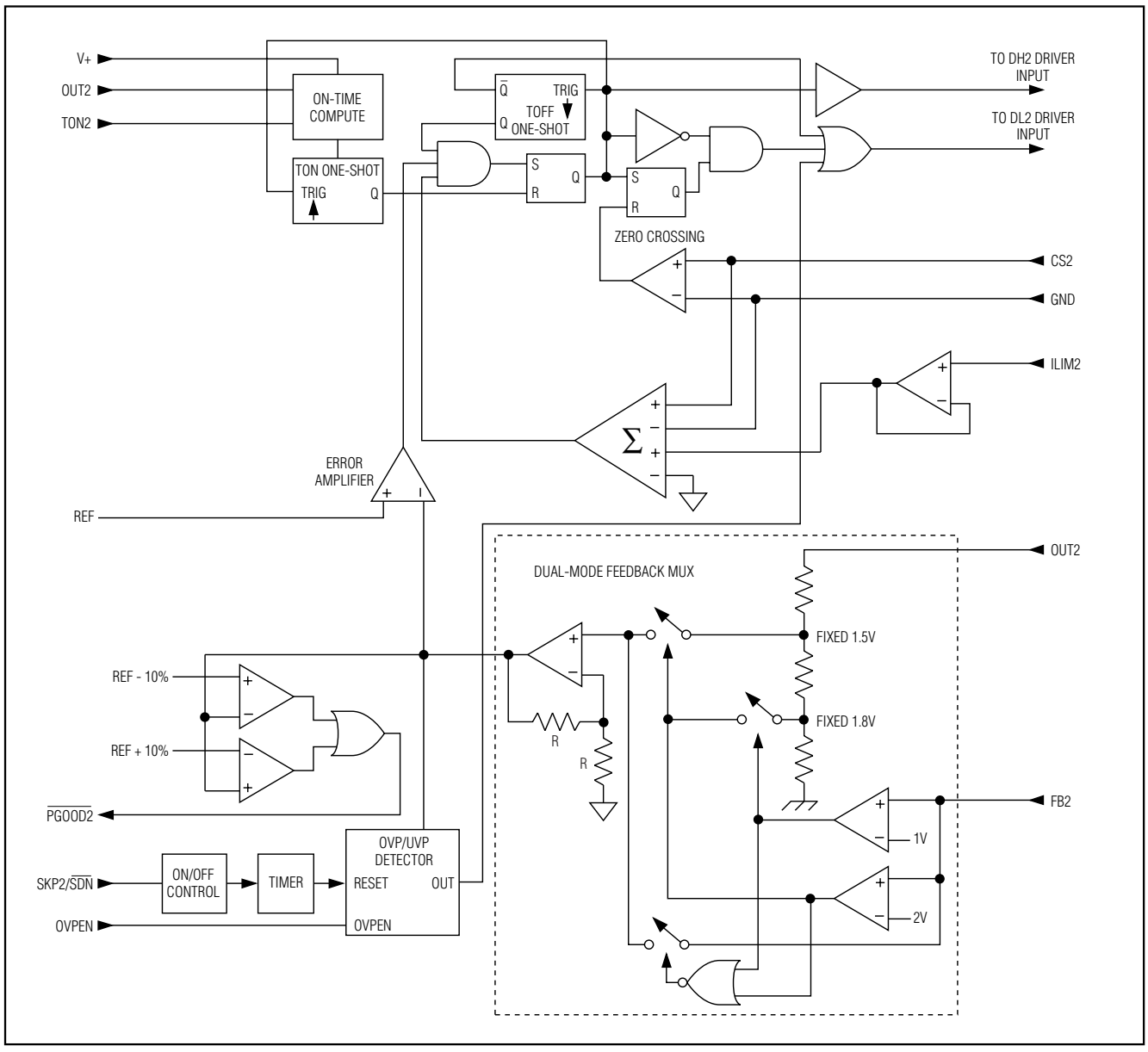


Figure 5. BUCK2 PWM Control Diagram

BUCK1 Integrator

BUCK1 includes a transconductance integrator (Figure 4) that provides a fine adjustment to the output regulation point. The integrator forces the DC average of the feedback voltage to equal the VID DAC setting. The circuit has the ability to lower the output voltage by 3% and raise it by 3%.

The differential input voltage range for the amplifier is at least ±60mV total, including DC offset and AC ripple. The integration time constant can be easily set with a capacitor at the CC pin. Use a capacitance of 47pF to 1000pF (47pF typ). The transconductance of the amplifier is 80µS (typ).

BUCK1 Differential Remote-Sense Amplifier (FBS, GDS)

The MAX1816/MAX1994 include differential remote-sense inputs to eliminate the effect of voltage drops down the PC board traces and through the processor's power leads. The FBS and GDS inputs enable true differential remote sense of the load voltage. The two inputs measure the voltage directly across the load to provide a signal that is summed with the feedback signals that set the voltage-positioned output. Connect the feedback sense input (FBS) directly to the positive load terminal and connect the ground sense input (GDS) directly to the negative load terminal. Modern microprocessors now include dedicated V_{CC} and ground-sense pins to facilitate the measurement of the chip's supply voltage.

BUCK1 Voltage-Positioning and Current-Sense Inputs (CS1+, CS1-)

The CS1+ and CS1- pins are differential inputs that measure the voltage drop across the sense resistor of BUCK1 for current-limiting, zero-crossing detection and active voltage positioning (Figure 4). The current-limit threshold is adjusted with an external resistive voltage-divider at ILIM1. A 10µA (min) divider current is recommended. The current-limit threshold adjustment range is from 25mV to 250mV. In adjustable mode, the current-limit threshold is precisely 1/10th of the voltage at ILIM1. The default current limit is 50mV when ILIM1 is connected to V_{CC}. The logic threshold for switchover to the default value is approximately V_{CC} - 1V.The default current limit accommodates the low voltage drop expected across the sense resistor.

The current-limit circuit of BUCK1 employs a unique "valley" current-sensing algorithm (Figure 6). If the magnitude of the current-sense voltage between CS1+ and CS1- is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and battery voltage.

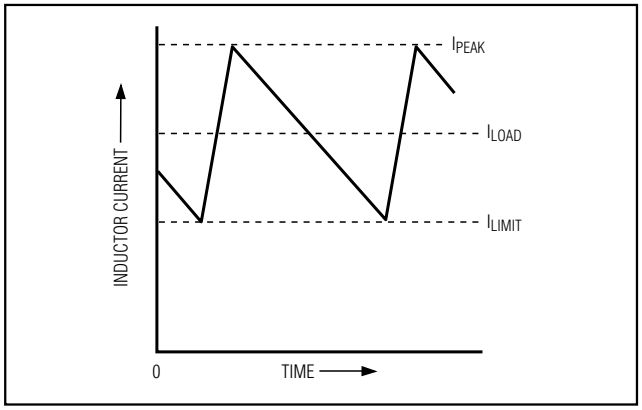


Figure 6. "Valley" Current-Limit Threshold Point

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT1} is sinking current in PWM mode.

The negative current-limit threshold is set to approximately 140% of the positive current limit and therefore tracks the positive current limit when ILIM1 is adjusted.

The GAIN pin controls the voltage-positioning gain. The slope of the output voltage as a function of load current is set by measuring the output current with a sense resistor (R_{SENSE}) in series with the inductor. An amplified version of this signal is fed back into the loop to decrease the output voltage. The required offset is added through the OFS0–OFS2 inputs (see the *BUCK1 Output-Voltage Offset Control* section). The exact relationship for the output of BUCK1 can be described with the following equation:

$$V_{OUT1} = V_{SET} - A_{VPS} \times (V_{CS1+} - V_{CS1-}) + V_{OS} \times SF$$

where V_{SET} is the programmed output voltage (see Tables 5 and 6), V_{OS} is the offset voltage generated from the selected OFS_ pin, SF is a scale factor (0.125) for the offset voltage, and A_{VPS} is the differential voltage-positioning gain set with the GAIN pin.

Since $V_{CS1+} - V_{CS1-} = I_{LOAD} \times R_{SENSE}$, substituting the differential sense voltage yields:

$$V_{OUT1} = V_{SET} - A_{VPS} \times I_{LOAD} \times R_{SENSE} + V_{OS} \times SF$$

The GAIN pin is a four-level logic input. When GAIN is set to GND, REF, open, and V_{CC}, the differential voltage gains are 0, 1.5, 2, and 4, respectively. Grounding GAIN disables the voltage-positioning function but does not disable the current limit.

BUCK2 Current-Sense Input (CS2)

BUCK2 uses the voltage at the CS2 pin to estimate the inductor current and determine the zero crossing for controlling pulse-skipping operation (Figure 5). Connect CS2 to the current-sense resistor (Figure 1) for the best possible current-limit accuracy. However, the improved accuracy is achieved at the expense of the additional power loss in the sense resistor. CS2 can be connected to LX2 for lossless current sensing. In this case, the trade-off is that the current limit becomes dependent on the low-side MOSFET's $R_{DS(ON)}$ with its inherent inaccuracies and thermal drift.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Like BUCK1, the current-limit circuit of BUCK2 also employs "valley" current sensing (Figure 6). If the magnitude of the current-sense voltage at CS2 is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and battery voltage.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT2} is sinking current in PWM mode. The negative current-limit threshold is set to approximately 140% of the positive current limit and therefore tracks the positive current limit when ILIM2 is adjusted.

The current-limit threshold is adjusted with an external resistive voltage-divider at ILIM2. A 10µA (min) divider current is recommended. The current-limit threshold adjustment range is from 25mV to 250mV. In adjustable mode, the current-limit threshold voltage is precisely 1/10th of the voltage at ILIM2. The threshold defaults to 50mV when ILIM2 is connected to V_{CC}. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V. The default current limit accommodates the low voltage drop expected across the sense resistor.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signal seen by CS2. Because CS2 is not a real differential current-sense input, minimize the return impedance from the sense resistor to the power ground to reduce voltage errors when measuring the current.

In Figure 1, the Schottky diode (D2) provides a current path parallel to the Q4/R2 current path. Accurate current sensing demands D2 to be off while Q4 conducts. Avoid large current-sense voltages. The combined voltage across Q4 and R2 can cause D2 to conduct. If very large sense voltages are used, connect D2 directly from Q4's source to drain.

Forced-PWM Mode

BUCK1 and BUCK2 operate in forced-PWM mode when SKP1/$\overline{SDN}$ and SKP2/$\overline{SDN}$ are unconnected. The low-noise forced-PWM mode disables the zero-crossing comparator, allowing the inductor current to reverse at light loads. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while DH_ maintains a duty factor of $V_{OUT\_}/V_{IN}$. The benefit of forced-PWM mode is to keep the switching frequency fairly constant, but it comes at a cost: the no-load 5V bias supply current can be 20mA to 80mA total for both BUCK1 and BUCK2, depending on the external MOSFETs and switching frequency.

Forced-PWM mode is most useful for reducing audio-frequency noise, improving load-transient response, providing sink-current capability for dynamic-output voltage adjustment, and improving the cross-regulation of multiple-output applications that use a flyback transformer or coupled inductor. BUCK1 uses PWM mode during all output transitions, while the slew-rate controller is active and for 32 clock cycles thereafter.

Automatic Pulse-Skipping Mode

In skip mode (SKP_/$\overline{SDN}$ = high), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical conduction" point).

In low duty-cycle applications, this threshold is relatively constant, with only a minor dependence on battery voltage.

$$I_{LOAD\_(SKIP)} = \frac{KV_{OUT\_}}{2L\_} \times \frac{V_{IN} - V_{OUT\_}}{V_{IN}}$$

where K is the on-time scale factor (Table 3). The load current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 7). For example, in the standard application circuit with K = 3.3µs (Table 3), V_{OUT1} = 1.25V, V_{IN} = 12V, and L1 = 0.68µH, switchover to pulse-skipping operation occurs at I_{LOAD1} = 2.7A. The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms can appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low-input-voltage levels.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

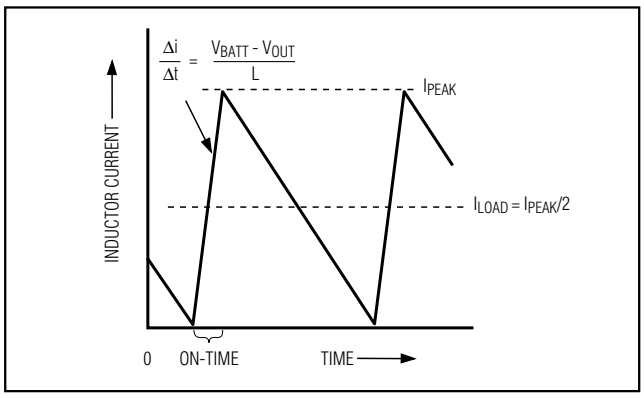


Figure 7. Pulse-Skipping/Discontinuous Crossover Point

DC output accuracy specifications for BUCK2 refer to the threshold of the error comparator. When the inductor is in continuous conduction, BUCK2 output voltage has a DC regulation level higher than the trip level by 50% of the ripple. In discontinuous conduction (SKP2/$\overline{SDN}$ = high, light-loaded), BUCK2 output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

Note that BUCK1 automatically enters forced-PWM mode during all output voltage transitions and stays in forced-PWM mode until the transition is completed and for 32 clock cycles thereafter. The reason for that is the forced-PWM operation provides current sinking capability required during output-voltage transitions.

Linear-Regulator Controller

The linear-regulator controller of the MAX1816/MAX1994 is an analog gain block with an open-drain N-channel output. It drives an external PNP pass transistor with a 220Ω base-to-emitter resistor (Figure 1). The controller is guaranteed to provide at least 20mA sink current. The linear regulator is typically used to provide a 1.2V/500mA VID logic supply. The controller is designed to be stable with an output capacitor of 10µF or more.

The output voltage can be adjusted with a resistive voltage-divider between the linear regulator output and analog ground with the center tap connected to LINFB. The set point of LINFB is 1.0V. The regulator is enabled when LIN/$\overline{SDN}$ is high. As soon as LINFB is in regulation, the open-drain power-good output LINGOOD goes high after a 1ms (min) delay. When the output goes out of regulation or LIN/$\overline{SDN}$ goes low, LINGOOD is forced low within approximately 10µs.

The 1ms (min) LINGOOD delay is necessary to allow the PLLs in the CPU to power up and stabilize before turning on the main regulator. The delay time is computed based on 1024 R_{TIME} clock cycles. As such, the delay varies based on the R_{TIME} period.

MOSFET Gate Drivers (DH_, DL_)

The DH_ and DL_ drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{IN} - $V_{OUT\_}$ differential exists. Two adaptive dead-time circuits monitor the DH_ and DL_ outputs and prevent the opposite side FET from turning on until DL_ or DH_ is fully off. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the adaptive dead-time circuits to work properly. Otherwise, the sense circuitry in the MAX1816/MAX1994 interprets the MOSFET gate as "off" while there is actually still charge left on the gate. Use very short, wide traces measuring 10 to 20 squares (50 mils to 100 mils wide if the MOSFET is 1in from the MAX1816/MAX1994).

The internal pulldown transistor that drives DL_ low is robust, with a very low pulldown resistance. For DL1, this resistance is 0.35Ω (typ), while the resistance for DL2 is slightly higher at 0.7Ω (typ). This helps prevent DL_ from being pulled up during the fast rise-time of the inductor node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, for high-current applications, some combinations of high- and low-side FETs can cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BST_, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 8).

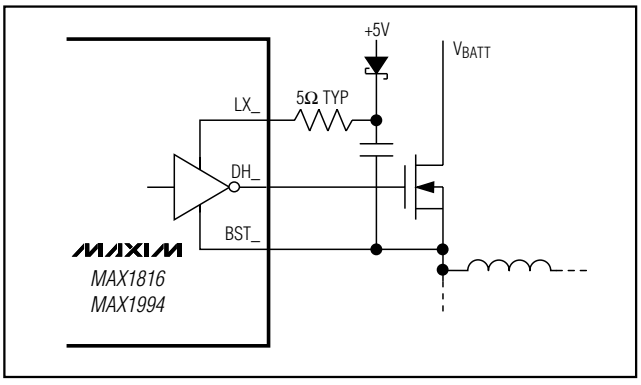


Figure 8. Reducing the Switching-Node Rise Time

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Shutdown Control (SKP1/$\overline{SDN}$, SKP2/$\overline{SDN}$, and LIN/$\overline{SDN}$)

If BUCK2 is used, always start BUCK2 before starting BUCK1. When SKP1/$\overline{SDN}$ goes below 0.5V, BUCK1 enters low-power shutdown mode. PGOOD goes low immediately. The output voltage ramps down to zero in 25mV steps at the clock rate set by R_{TIME}. Thirty-two clocks after the DAC reaches the zero setting, DL1 is forced to V_{DD}, and DH1 is forced low. When SKP1/$\overline{SDN}$ goes above 1.4V or floats, the DAC target is evaluated and switching begins. The slew-rate controller ramps up from zero in 25mV steps to the selected DAC code value. There is no traditional soft-start (variable current-limit) circuitry, so full output current is available immediately. Floating SKP1/$\overline{SDN}$ causes BUCK1 to operate in low-noise forced-PWM mode. Forcing SKP1/$\overline{SDN}$ above 2.8V enables skip mode operation.

When SKP2/$\overline{SDN}$ goes below 0.5V, BUCK2 enters shutdown mode. In shutdown mode, DL2 is forced to V_{DD} if overvoltage protection is enabled. If OVPSET is connected to V_{CC}, overvoltage protection is disabled and DL2 is forced low in shutdown mode.

When LIN/$\overline{SDN}$ goes below 0.8V, the linear regulator of the MAX1816/MAX1994 enters shutdown mode. In shutdown mode, LINBSE is forced to a high-impedance state preventing sufficient drive to the external PNP pass transistor in the regulator. LINGOOD is forced low within 10µs (typ) when LIN/$\overline{SDN}$ goes low. Forcing LIN/$\overline{SDN}$ above 2.4V turns on the linear regulator.

Power-On Reset

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the MAX1816/MAX1994 for operation. V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching, forces PGOOD low, and forces the DL1 gate driver high (to enforce output overvoltage protection). The DL2 gate driver is also forced high if OVP is enabled. When V_{CC} rises above 4.25V, the DAC inputs are sampled and the output voltage begins to slew to the DAC setting. For automatic startup, the battery voltage should be present before V_{CC}. If the MAX1816/MAX1994 attempt to bring the output into regulation without the battery voltage present, the fault latch will trip. Toggling any of the shutdown control pins resets the fault latch.

Power Valid Outputs (PGOOD and LINGOOD)

PGOOD is an open-drain power-good output. Table 4 describes the behavior of PGOOD with respect to the logic inputs. Window comparators on FBS and OUT2 (FB2) control the PGOOD output. If BUCK1 and BUCK2 are in regulation then PGOOD is high, except during power-up and power-down.

The PGOOD output goes low if FBS or OUT2 (FB2) is outside a window of ±10% about the nominal set point (see the *DAC Inputs and Internal Multiplexers* and *Adjusting BUCK2 Output Voltage* sections).

PGOOD is forced low when SKP1/$\overline{SDN}$ is low. If SKP2/$\overline{SDN}$ is low, then OUT2 (FB2) does not affect PGOOD. Normally, PGOOD is forced high during all VID transitions, and stays high for 4 clock periods after the DAC count is equalized. If BUCK2 goes out of regulation during these conditions, then PGOOD goes low as a consequence. A pullup resistor on PGOOD causes additional finite shutdown current.

The following conditions must all be met for PGOOD to go high:

- V_{CC} must be above UVLO.
- SKP1/$\overline{SDN}$ must be greater than 1.4V or unconnected.
- The output of BUCK1 must be within a window of ±10% about the nominal set point.
- PGOOD is forced high during DAC code transitions of BUCK1. The “blanking” period persists for N+4 R_{TIME} clock cycles. Blanking does not occur during power-up and power-down.
- If SKP2/$\overline{SDN}$ is not low, then OUT2 (FB2) must be within a window of ±10% about the nominal set point.
- When enabled, a fault on OUT2 overrides the blanking on BUCK1.

LINGOOD is an open-drain power-good output for the linear regulator. LINGOOD goes high at least 1ms after the internal comparator signals that the output is in regulation. In normal operation, if the internal comparator signals that the circuit is out of regulation, LINGOOD goes low within approximately 10µs (typ). If LIN/$\overline{SDN}$ goes low, LINGOOD is immediately forced low.

Note that all three regulators are forced off when a fault is detected. DL_ are forced high, DH_ are forced low, and the linear regulator is turned off. (See the *Output Overvoltage Protection, Output Undervoltage Protection, UVLO,* and *Thermal Fault Protection* sections).

DAC Inputs and Internal Multiplexers (SUS)

The MAX1816/MAX1994 have a unique internal VID input multiplexer (mux) that can select one of two different VID DAC code settings for different processor states. When the logic level at SUS is low, the mux selects the VID DAC code settings from the D0–D4 inputs (Table 5). Do not leave D0–D4 floating—use 100kΩ pullup resistors if the inputs float. When SUS is high, the suspend mode mux selects the VID DAC code settings from the S0/S1 input decoder. The outputs of the decoder are determined by

Table 4. BUCK1 and BUCK2 Operating Mode Truth Table

OVP	SKP1/$\overline{SDN}$	SKP2/$\overline{SDN}$	DL1	DL2	MODE	PGOOD
X	GND	V_{CC}	HIGH	Switching	BUCK2	LOW
Enabled	V_{CC}	GND	Switching	HIGH	BUCK1	Monitor BUCK1 only
Disabled	V_{CC}	GND	Switching	LOW	BUCK1	Monitor BUCK1 only
Enabled	GND	GND	HIGH	HIGH	Shutdown	LOW
Disabled	GND	GND	HIGH	LOW	Shutdown	LOW
X	V_{CC}	V_{CC}	Switching	Switching	Both in skip mode	Monitor both
Enabled	>10.8V	GND	Switching	HIGH	BUCK1 no-fault test mode	Monitor BUCK1 only
Disabled	>10.8V	GND	Switching	LOW	BUCK1 no-fault test mode	Monitor BUCK1 only
X	>10.8V	V_{CC}	Switching	Switching	No-fault test mode	Monitor both
X	>10.8V	Float	Switching	Switching in forced PWM mode	No-fault test mode	Monitor both
Enabled	Float	GND	Switching in forced PWM mode	HIGH	BUCK1 in forced PWM mode	Monitor BUCK1 only
Disabled	Float	GND	Switching in forced PWM mode	LOW	BUCK1 in forced PWM mode	Monitor BUCK1 only
X	Float	V_{CC}	Switching in forced PWM mode	Switching	BUCK1 in forced PWM mode, BUCK2 in skip mode	Monitor both
X	Float	Float	Switching in forced PWM mode	Switching in forced PWM mode	BUCK1 and BUCK2 in forced PWM Mode	Monitor both
X	GND	Float	HIGH	Switching in forced PWM mode	BUCK1 off, BUCK in forced PWM mode	LOW
X	V_{CC}	Float	Switching	Switching in forced PWM mode	BUCK1 in skip mode, BUVK2 in forced PWM mode	Monitor both
Enabled	V_{CC} or float	V_{CC} or float	HIGH	HIGH	OVP and UVP faults	LOW
Disabled	V_{CC} or float	V_{CC} or float	HIGH	HIGH	UVP faults only	LOW

X = Don't care.

inputs S0 and S1, which are four-level digital inputs (Table 6). All code transitions (even those asking for the exact same code) activate the slew-rate controller. In other words, up-going or down-going transitions from one code to another, soft-start and soft-stop are all handled in the same way.

BUCK1 Output-Voltage Offset Control (SUS, PERF, $\overline{DPSLP}$, and OFS_)

The MAX1816/MAX1994 support three independent offsets to the voltage-positioned load line. The offsets are adjusted using resistive voltage-dividers at the OFS0–OFS2 inputs (see Figure 10). For inputs from 0 to 0.8V, a negative offset is added to the output that is

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Table 5. Output Voltage vs. DAC Codes

D4	D3	D2	D1	D0	V_{OUT} (V) MAX1816	V_{OUT} (V) MAX1994
0	0	0	0	0	1.750	2.000
0	0	0	0	1	1.700	1.950
0	0	0	1	0	1.650	1.900
0	0	0	1	1	1.600	1.850
0	0	1	0	0	1.550	1.800
0	0	1	0	1	1.500	1.750
0	0	1	1	0	1.450	1.700
0	0	1	1	1	1.400	1.650
0	1	0	0	0	1.350	1.600
0	1	0	0	1	1.300	1.550
0	1	0	1	0	1.250	1.500
0	1	0	1	1	1.200	1.450
0	1	1	0	0	1.150	1.400
0	1	1	0	1	1.100	1.350
0	1	1	1	0	1.050	1.300
0	1	1	1	1	1.000	No CPU
1	0	0	0	0	0.975	1.275
1	0	0	0	1	0.950	1.250
1	0	0	1	0	0.925	1.225
1	0	0	1	1	0.900	1.200
1	0	1	0	0	0.875	1.175
1	0	1	0	1	0.850	1.150
1	0	1	1	0	0.825	1.125
1	0	1	1	1	0.800	1.100
1	1	0	0	0	0.775	1.075
1	1	0	0	1	0.750	1.050
1	1	0	1	0	0.725	1.025
1	1	0	1	1	0.700	1.000
1	1	1	0	0	0.675	0.975
1	1	1	0	1	0.650	0.950
1	1	1	1	0	0.625	0.925
1	1	1	1	1	0.600	No CPU

equal to 1/8th the voltage appearing at the selected OFS input (ΔV_{OUT} = -0.125 × $V_{OFS\_}$). For inputs from 1.2V to 2V, a positive offset is added to the output that is equal to 1/8th the difference between the reference voltage and the voltage appearing at the selected OFS input (ΔV_{OUT} = 0.125 × (V_{REF} - $V_{OFS\_}$)). With this scheme, both positive and negative offsets can be achieved with a single voltage-divider. The piecewise linear transfer function is shown in Figure 9.

Table 6. Output Voltage vs. Suspend Mode DAC Codes

S1	S0	V_{OUT} (V) MAX1816/MAX1994
GND	GND	1.075
GND	REF	1.050
GND	OPEN	1.025
GND	V_{CC}	1.000
REF	GND	0.975
REF	REF	0.950
REF	OPEN	0.925
REF	V_{CC}	0.900
OPEN	GND	0.875
OPEN	REF	0.850
OPEN	OPEN	0.825
OPEN	V_{CC}	0.800
V_{CC}	GND	0.775
V_{CC}	REF	0.750
V_{CC}	OPEN	0.725
V_{CC}	V_{CC}	0.700

The regions of the transfer function below zero, above 2.0V, and between 0.8V and 1.2V are undefined. OFS inputs are disallowed in these regions, and the respective effects on the output are not specified.

The offset control inputs are selected using a combination of the three logic inputs (SUS, PERF, and $\overline{DPSLP}$), which also define the operating mode for the MAX1816/MAX1994. Table 7 details which OFS input is selected based on these control inputs.

BUCK1 Output-Voltage Transition Timing

The MAX1816/MAX1994 are designed to perform output voltage transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the regulator to perform nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance.

Modern mobile CPUs operate at multiple clock frequencies that require multiple VID settings. It is common when transitioning from one clock frequency to another for the CPU to go into a low-power state before changing the output voltage and clock frequency. The change must be accomplished within a fixed time interval—often less than 100µs.

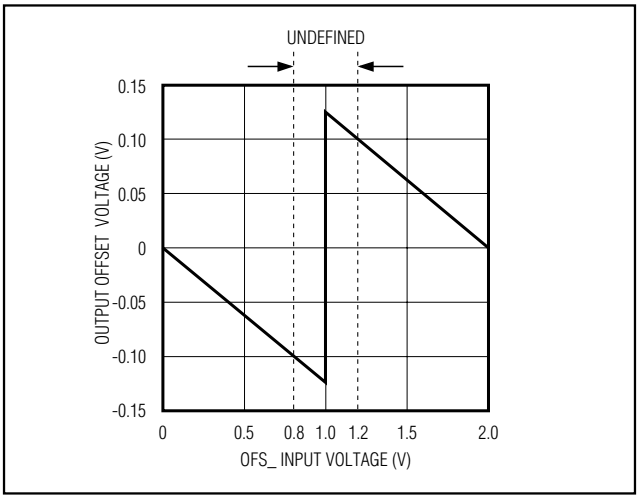


Figure 9. Offset-Control Transfer Function

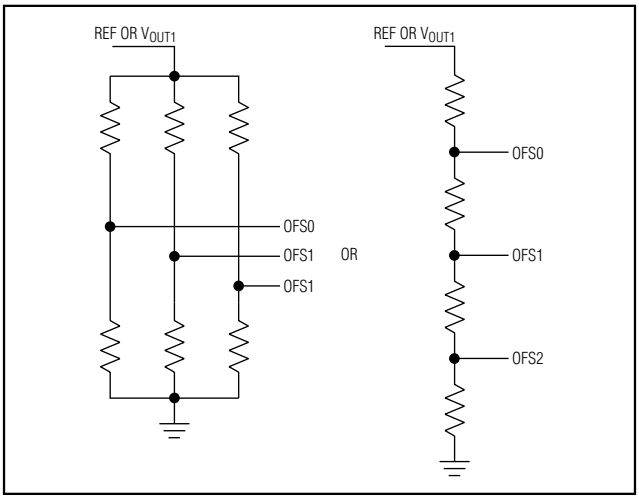


Figure 10. Simplified Offset-Control Circuits

At the beginning of an output voltage transition, the regulator is placed in forced-PWM mode and the PGOOD output is high. If there is a fault on BUCK2 during this period, PGOOD goes low. The output voltage follows the internal DAC code, which changes in 25mV increments until it reaches the programmed VID code. The regulator remains in forced-PWM mode for 32 clock cycles after the transition to ensure that the output settles properly. The PGOOD output is forced high for 4 clock cycles after the transition also to allow the output to settle. The slew-rate clock frequency (set by the R_{TIME} resistor) must be set fast enough to ensure that the longest transition is completed within the allotted time interval.

The output voltage transition is performed in 25mV steps, preceded by a 4µs delay and followed by one additional clock period. The total time for a transition depends on R_{TIME}, the voltage difference, and the accuracy of the MAX1816/MAX1994s' slew-rate clock, and is not dependent on the total output capacitance. The greater the output capacitance, the higher the surge current required for the transition. The MAX1816/MAX1994 automatically control the current to the minimum level required to complete the transition in the calculated time. As long as the surge current is less than the current limit set by ILIM1, the transition time is given by:

$$t_{SLEW} \le 4\mu s + \left[\frac{1}{f_{SLEW}}\left(1 + \frac{V_{OLD} - V_{NEW}}{25mV}\right)\right]$$

where f_{SLEW} = 252kHz × 143kΩ / R_{TIME}, V_{OLD} is the original DAC setting, and V_{NEW} is the new DAC setting. See Time Frequency Accuracy in the *Electrical Characteristics* table for f_{SLEW} accuracy. The practical range of R_{TIME} is 68kΩ to 680kΩ, corresponding to 1.9µs to 19µs per 25mV step. Although the DAC takes discrete 25mV steps, the output filter makes the transitions relatively smooth. The average inductor current required to make an output voltage transition is:

$$I_L \cong C_{OUT} \times 25mV \times f_{SLEW}$$

The slew-rate controller also performs a soft-start and soft-stop function. The soft-start function works by counting up from zero, in order to minimize turn-on surge currents. The soft-stop executes this process in reverse, eliminating the negative output voltages and the need for an external Schottky output clamp diode that would otherwise be required if DL1 were simply forced high.

Setting BUCK2 Output Voltage

BUCK2's Dual Mode™ operation allows the selection of common voltages without requiring external components (Figure 1). In fixed mode, connect FB2 to AGND for 2.5V output, or connect FB2 to V_{CC} for 1.8V output. In adjustable mode, the output voltage can be adjusted from 1.0V to 5.5V using a resistive voltage-divider from the BUCK2 output to AGND with the center tap connected to FB2 (Figure 11). The equation for adjusting the output voltage is:

$$V_{OUT2} = V_{FB2}\left(1 + \frac{R1}{R2}\right)$$

where V_{FB2} is 1.0V.

Dual Mode is a trademark of Maxim Integrated Products, Inc.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Table 7. Offset Selection Truth Table

MODE	INPUTS			ACTIVE OFS INPUTS		
	SUS	PERF	$\overline{DPSLP}$	OFS2	OFS1	OFS0
Battery Sleep	0	0	0	1	0	0
Battery	0	0	1	0	1	0
Performance Sleep	0	1	0	0	0	1
Performance	0	1	1	0	0	0
Suspend	1	0	0	0	0	0
Suspend	1	0	1	0	0	0
Suspend	1	1	0	0	0	0
Suspend	1	1	1	0	0	0

0 = Logic low or input not selected.
1 = Logic high or input selected.

Output Overvoltage Protection

Output overvoltage protection (OVP) is available on BUCK1, BUCK2, and the linear regulator. The LINFB input is always monitored for overvoltage. The FBS and OUT2 inputs are only monitored for overvoltages when OVP is enabled. When any output exceeds the desired OVP threshold, the fault latch is set and the regulator is turned off. In the fault mode, DL1 and DL2 are forced high, DH1 and DH2 are forced low, and the linear regulator is turned off. For BUCK1 and BUCK2, if the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse will blow. DL1 is also kept high continuously when V_{CC} UVLO is active, as well as in shutdown mode (Table 4). The device remains in the fault mode until V_{CC} is cycled, or either SKP_/$\overline{SDN}$ or LIN/$\overline{SDN}$ is toggled. The triggering of the reset condition occurs on the rising edge of the SKP_/$\overline{SDN}$ or LIN/$\overline{SDN}$ signals.

For BUCK1, the default OVP threshold is 2V for the MAX1816 and 2.25V for the MAX1994. For BUCK2, the OVP threshold is 115% of the nominal voltage for OUT2 (FB2 if external feedback is used for BUCK2). The overvoltage detection level for FBS can be adjusted through an external resistive voltage-divider. Connecting OVPSET to a voltage between 1.0V and 2.0V sets the OVP threshold for FBS. For the MAX1816, the fault latch is set when $V_{FBS} > V_{OVPSET}$. For the MAX1994, the fault latch is set when $V_{FBS} > 1.125 \times V_{OVPSET}$. The OVP threshold on OUT2 is not adjustable and remains at the default value of 115%. Connecting OVPSET to V_{CC} disables OVP for BUCK1 and BUCK2. The operation of the linear regulator is not affected by OVPSET. Overvoltage protection can be disabled using the NO FAULT test mode (see the *NO FAULT Test Mode* section).

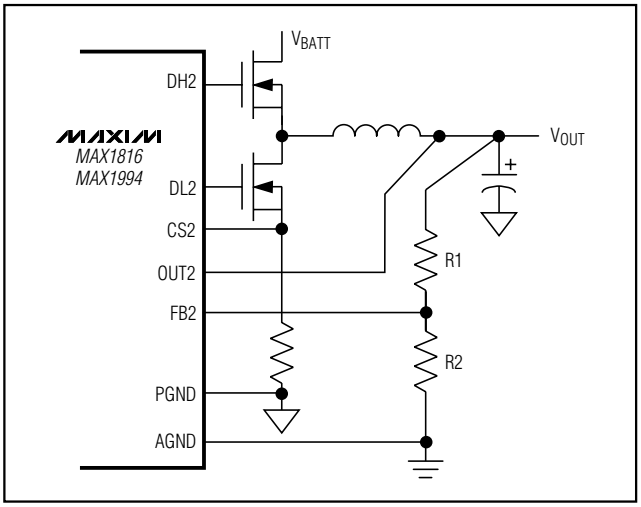


Figure 11. Adjusting BUCK2 Output Voltage with a Resistive Voltage-Divider

Output Undervoltage Protection

The output undervoltage protection (UVP) is available on BUCK1, BUCK2, and the linear regulator. The protection is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the output voltage is under 70% of the nominal value for BUCK1 and BUCK2, and under 90% for the linear regulator (see the *Electrical Characteristics* table for the respective UVP thresholds), the fault latch is set. In the fault mode, DL1 and DL2 are forced high, DH1 and DH2 are forced low, and the linear regulator is turned off. The controller does not restart until V_{CC} power is cycled, or either SKP_/$\overline{SDN}$ or LIN/$\overline{SDN}$ is toggled. The triggering of the reset condition occurs on the rising edge of the SKP_/$\overline{SDN}$ or LIN/$\overline{SDN}$ signals.

To allow startup, UVP is ignored during the undervoltage blanking time (the first 256 cycles of the slew rate after startup for BUCK1, the first 4096 cycles for BUCK2 and the first 512 cycles for the linear regulator). UVP can be disabled using the NO FAULT test mode (see the *NO FAULT Test Mode* section).

UVLO

The MAX1816/MAX1994 provide input undervoltage lockout (UVLO) protection. If the V_{CC} voltage drops low enough to trip the UVLO comparator, it is assumed that there is not enough supply voltage to make valid decisions. In order to protect the output from overvoltage faults, DL1 and DL2 are forced high if OVP is enabled, DH_ is forced low, and the linear regulator is turned off. If OVP is disabled, DL1 is forced high, DL2 is forced low, DH_ is forced low, and the linear regulator is turned off. For BUCK1 (and also for BUCK2 if OVP is enabled), this condition rapidly forces the outputs to zero since the slew-rate controller is not active. The fault results in large negative inductor currents and possibly small negative output voltages. If V_{CC} is likely to drop in this fashion, the outputs can be clamped with Schottky diodes to PGND to reduce the negative excursions.

Thermal Fault Protection

The MAX1816/MAX1994 feature a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latch, which pulls DL_ high, DH_ low, and turns off the linear regulator. The device remains in fault mode until the junction temperature cools by 15°C, and either V_{CC} power is cycled, or SKP_/$\overline{SDN}$ or LIN/$\overline{SDN}$ is toggled.

NO FAULT Test Mode

The over/undervoltage protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a test mode is provided to disable the OVP, UVP, and thermal shutdown features, and clear the fault latch if it has been set. Test mode applies to BUCK1, BUCK2, and the linear regulator. In the test mode, BUCK1 operates as if SKP1/$\overline{SDN}$ was high (skip mode). Set the voltage on SKP1/$\overline{SDN}$ between 10.8V to 13.2V to enable the NO FAULT test mode.

BUCK1/BUCK2 Design Procedure

Firmly establish the input voltage range and maximum load current for BUCK1 and BUCK2 before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

1) **Input Voltage Range.** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice, lower input voltages result in better efficiency.

2) **Maximum Load Current.** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

3) **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

4) **Inductor Operating Point.** This choice provides tradeoffs between size and efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The MAX1816/MAX1994s' pulse-skipping algorithm initiates skip mode at the critical conduction point. So, the inductor operating point also determines the load current value at which PFM/PWM switchover occurs. The optimum point is usually found between 20% and 50% ripple current.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

5) **Inductor Ripple Current.** The inductor ripple current also impacts transient response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{(I_{LOAD1} - I_{LOAD2})^2 \times L \times \left(K\frac{V_{OUT}}{V_{IN}} + t_{OFF(MIN)}\right)}{2 \times C_{OUT} \times V_{OUT} \times \left[K\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* table) and K is from Table 3.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times LIR \times I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)}$ = 19A, V_{IN} = 7V, V_{OUT} = 1.25V, f_{SW} = 300kHz, 30% ripple current or LIR = 0.30:

$$L = \frac{1.25V \times (7V - 1.25V)}{7V \times 300kHz \times 0.30 \times 19A} = 0.60\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{LIR}{2}\right)$$

Setting the Current Limit for BUCK1

Connect ILIM1 to V_{CC} for a default 50mV (CS1+ to CS1-) current-limit threshold. For an adjustable threshold, connect a resistive voltage-divider from REF to GND, with ILIM1 connected to the center tap. The current-limit threshold is precisely 1/10th of the voltage at ILIM1. When adjusting the current limit, use 1% tolerance resistors for the divider and a 10µA divider current to prevent a significant increase of errors in the current-limit threshold.

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current; therefore:

$$I_{LIMIT(MIN)} > I_{LOAD(MAX)} \times \left(1 - \frac{LIR}{2}\right)$$

The current-sense resistor value (R1 in Figure 1) is calculated according to the worst-case (minimum) current-limit threshold voltage (see the *Electrical Characteristics* table) and the valley current-limit threshold $I_{LIMIT(MIN)}$ described above:

$$R_{SENSE} = \frac{50mV \times 0.8}{I_{LIMIT(MIN)}} \quad \text{(Fixed Mode)}$$

$$R_{SENSE} = \frac{V_{ILIM1} \times 0.1 \times 0.8}{I_{LIMIT(MIN)}} \quad \text{(Adjustable Mode)}$$

where 0.8 is a factor for the worst-case low current-limit threshold.

To protect against component damage during short-circuit conditions, use the calculated value of R_{SENSE} to size the MOSFET switches and specify inductor saturation-current ratings according to the worst-case high current-limit threshold:

$$I_{PEAK(MAX)} = \frac{50mV \times 1.2}{R_{SENSE}} \times (1 + LIR)$$

(Fixed Mode)

$$I_{PEAK(MAX)} = \frac{V_{ILIM1} \times 0.1 \times 1.2}{R_{SENSE}} \times (1 + LIR)$$

(Adjustable Mode)

where 1.2 is a factor for worst-case high current-limit threshold.

Low-inductance resistors, such as surface-mount metal film, are recommended.

Setting the Current Limit for BUCK2

Connect ILIM2 to V_{CC} for a default 50mV CS2 to GND current-limit threshold. For an adjustable threshold, connect a resistive voltage-divider from REF to GND, with ILIM2 connected to the center tap. The current-limit threshold is precisely 1/10th of the voltage at ILIM2. When adjusting the current limit, use 1% tolerance resistors for the divider and a 10µA divider current to prevent a significant increase of errors in the current-limit threshold.

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current; therefore:

$$I_{LIMIT(MIN)} > I_{LOAD(MAX)} \times \left(1 - \frac{LIR}{2}\right)$$

where $I_{LIMIT(MIN)}$ equals the minimum current-limit threshold voltage divided by the current-sense resistor.

The sense resistor (R2 in Figure 1) determines the achievable current-limit accuracy. There is a trade-off between current-limit accuracy and sense-resistor power dissipation. Most applications employ a current-sense voltage of 50mV to 100mV. Choose a sense resistor so that:

$$R_{SENSE} = \frac{50mV \times 0.8}{I_{LIMIT(MIN)}} \quad \text{(Fixed Mode)}$$

$$R_{SENSE} = \frac{V_{ILIM2} \times 0.1 \times 0.8}{I_{LIMIT(MIN)}} \quad \text{(Adjustable Mode)}$$

where 0.8 is a factor for worst-case low current-limit threshold.

Extremely cost-sensitive applications that do not require high-accuracy current sensing can use the on-resistance of the low-side MOSFET switch in place of the sense resistor by connecting CS2 to LX2. Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET data sheet taking into account the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C temperature rise.

Assume the current-sense resistor in the application circuit in Figure 1 is removed and CS2 is directly tied to LX2. The Q4 maximum $R_{DS(ON)}$ = 3.8mΩ at T_J = +25°C and 5.7mΩ at T_J = +125°C.

The minimum current-limit threshold is:

$$I_{LIMIT(MIN)} = \frac{500mV \times 0.1 \times 0.8}{5.7m\Omega} = 7A$$

and the required valley current limit is:

$$I_{LIMIT(MIN)} > 7A \times (1 - 0.30/2) = 5.95A$$

since 7A is greater than the required 5.95A, the circuit can deliver the 7A full-load current.

Output Capacitor Selection (BUCK1 and BUCK2)

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

In CPU core voltage regulators and other applications where the output is subject to violent load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{DIP}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output-voltage ripple:

$$R_{ESR} \le \frac{V_{P-P}}{LIR \times I_{LOAD(MAX)}}$$

The actual microfarad capacitance value required often relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OSCONs, and other electrolytics).

When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem.

The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} = \frac{L \times I_{PEAK}^2}{2 \times C_{OUT} \times V_{OUT}}$$

where I_{PEAK} is the peak inductor current.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

BUCK1 Stability Considerations

BUCK1 is fundamentally different from previous Quick-PWM controllers in two respects: it uses a current-sense amplifier to obtain the current feedback signal (ramp), and it uses differential remote sense to compensate for voltage drops along the high-current path. The regulator adds the differential remote-sense signal to the current-feedback signal to correct the output voltage. As long as the amplitude of the resulting signal is greater than 1% of the output voltage, the regulator remains stable. Stability can be determined by comparing the zero formed with the current-sense feedback network to the switching frequency.

The boundary condition of stability is given by the following expression:

$$f_Z \le \frac{f_{SW}}{\pi}$$

$$f_Z \approx \frac{1}{2\pi \times \left[\begin{array}{l} R_{DROOP} \times (C_{OUT1} + C_{REMOTE}) + \\ R_{LOCAL} \times C_{OUT1} + R_{REMOTE} \times C_{REMOTE} \end{array} \right]}$$

where C_{OUT1} is the local output capacitance (Figure 1), C_{REMOTE} is the remote output capacitance, R_{LOCAL} is the ESR of the local capacitors, R_{REMOTE} is the ESR of the remote capacitors, and R_{DROOP} is the effective voltage-positioning resistance, which is determined by the voltage-positioning gain A_{VPS} and current-sense resistor R_{SENSE}:

$$R_{DROOP} = A_{VPS} \times R_{SENSE}$$

Like previous Quick-PWM controllers, larger values of ESR and sense resistance increase stability. The voltage-positioning gain A_{VPS} effectively increases the sense resistance, which further enhances stability.

The RC time constants of the local and remote capacitors affect the stability criteria. These two time constants are defined as follows:

$$\tau_{LOCAL} = (R_{DROOP} + R_{LOCAL} + R_{PCB\_TRACE}) \times C_{OUT1}$$

$$\tau_{REMOTE} = (R_{DROOP} + R_{REMOTE}) \times C_{REMOTE}$$

where R_{PCB_TRACE} is the PC board trace resistance shown in Figure 1.

When the local capacitance time constant is either much greater or much smaller than that of the remote capacitance, the stability criteria is:

$$R_{DROOP} \times (C_{OUT1} + C_{REMOTE}) + R_{LOCAL} \times C_{OUT1} + R_{REMOTE} \times C_{REMOTE} \ge \frac{1}{2 \times f_{SW}}$$

In applications where these two time constants are approximately equal, the criteria for stable operation reduces to:

$$(R_{DROOP} + R_{LOCAL}) \times C_{OUT1} \ge \frac{1}{2 \times f_{SW}} \text{ and}$$

$$(R_{DROOP} + R_{REMOTE}) \times C_{REMOTE} \ge \frac{1}{2 \times f_{SW}}$$

The standard application circuit (Figure 1) operating at 300kHz easily achieves stable operation because the time constant of the local capacitors is much greater than that of the remote capacitors.

In this example, C_{OUT1} = 990µF, R_{LOCAL} = 3.3mΩ, C_{REMOTE} = 10µF, R_{REMOTE} = 5mΩ, and R_{DROOP} = 2 x 1mΩ = 2mΩ:

$$2m\Omega \times (990\mu F + 10\mu F) + 3.3m\Omega \times 990\mu F + 5m\Omega \times 10\mu F \ge \frac{1}{2 \times 300kHz}$$

$$5.32\mu s \ge 1.67\mu s$$

When voltage positioning is not used (A_{VPS} = 0) and the ESR of the output capacitors alone cannot meet the stability requirement, the current feedback signal must be generated from a different source. The current ramp signal at CS1+ and the output voltage must be summed at the FBS input. For stable operation, a 3.3µF feed-forward capacitor is added from the CS1+ input to FBS and a 10Ω resistor is inserted from the remote load to FBS forming an RC filter (Figure 12). The cutoff frequency of the RC filter should be approximately an order of magnitude lower than the regulator's switching frequency to prevent sluggish transient response. To avoid input-bias current-induced offset errors, the resistor should be less than 20Ω.

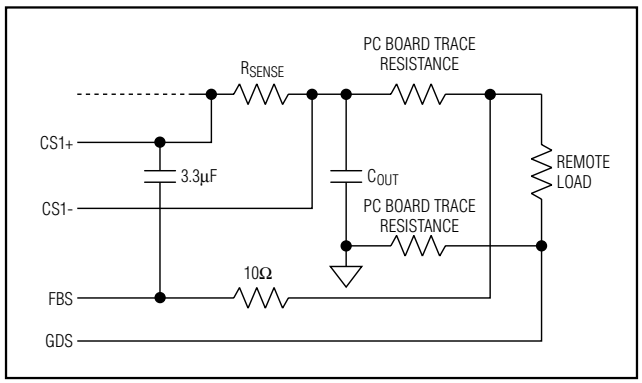


Figure 12. Output Feed Forward for Nonvoltage-Positioned Applications

For nonvoltage-positioned applications using a feed-forward circuit, the RC time constants of the local and remote capacitors are defined as:

$$\tau_{LOCAL} = (R_{SENSE} + R_{LOCAL}) \times C_{OUT1}$$

$$\tau_{REMOTE} = (R_{SENSE} + R_{REMOTE} + R_{PCB\_TRACE}) \times C_{REMOTE}$$

The new stability criteria for nonvoltage-positioned applications using feed forward becomes:

$$R_{SENSE} \times (C_{OUT1} + C_{REMOTE}) + R_{LOCAL} \times C_{OUT1} + R_{REMOTE} \times C_{REMOTE} \geq \frac{1}{2 \times f_{SW}}$$

for τ_{LOCAL} much greater or much smaller than τ_{REMOTE}, and

$$(R_{SENSE} + R_{LOCAL}) \times C_{OUT1} \geq \frac{1}{2 \times f_{SW}} \text{ and}$$

$$(R_{SENSE} + R_{REMOTE}) \times C_{REMOTE} \geq \frac{1}{2 \times f_{SW}}$$

when τ_{LOCAL} and τ_{REMOTE} are approximately equal.

If the voltage-positioning gain in the standard application circuit (Figure 1) is set to zero and the feed-forward compensation circuit shown in Figure 12 is used, stable operation can still be easily achieved.

In this example, C_{OUT1} = 990µF, R_{LOCAL} = 3.3mΩ, C_{REMOTE} = 10µF, R_{REMOTE} = 5mΩ, R_{SENSE} = 1mΩ, and R_{PCB_TRACE} = 2mΩ, and the local time constant is much greater than the remote time constant.

Therefore:

$$1m\Omega \times (990\mu F + 10\mu F) + 3.3m\Omega \times 990\mu F + 5m\Omega \times 10\mu F \geq \frac{1}{2 \times 300kHz}$$

$$4.32\mu s \geq 1.67\mu s$$

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output-voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient current feedback signal.

Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit. The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

BUCK2 Stability Considerations

The stability criterion for BUCK2 is the same as previous Quick-PWM controllers like the MAX1714. Stability is determined by comparing the value of the ESR zero to the switching frequency. The point of stability is given by the following expression:

$$f_{ESR} \leq \frac{f_{SW}}{\pi}$$

where $$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

For good phase margin, it is recommended to increase the equivalent RC time constant by a factor of two. The standard application circuit (Figure 1) operating at 390kHz with C_{OUT} = 330µF and R_{ESR} = 10mΩ, easily meets this requirement.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = I_{LOAD} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

The RMS input currents for BUCK1 and BUCK2 can be calculated using the above equation. Use the sum of these two currents as the total RMS current. Note that this is a very conservative estimation because the two regulators are never in phase 100% of the time. The actual RMS current is always lower than the calculated value.

For most applications, nontantalum chemistries (ceramic or OSCON) are preferred due to their resilience to inrush surge currents typical of systems with a switch or a connector in series with the battery. If the MAX1816/MAX1994 operate as the second stage of a two-stage power conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability (>12A) when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (Q1 in Figure1) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of Q1. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of Q1. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET (Q2) that has the lowest possible $R_{DS(ON)}$, comes in a moderate-sized package (i.e., two or more 8-pin SOs, DPAKs, or D^2PAKs), and is reasonably priced. Ensure that the MAX1816/MAX1994 DL_ gate driver can drive Q2; in other words, check that the dV/dt caused by Q1 turning on does not pull up the gate of Q2 due to drain-to-gate capacitance, causing cross-conduction problems. Switching losses are not an issue for the low-side MOSFET, since it is a zero-voltage switched device when used in the buck topology.

MOSFET Power Dissipation

The high-side MOSFET conduction power dissipation due to on-state channel resistance is:

$$PD(Q1\_Conduction) = \frac{V_{OUT}}{V_{IN}} \times I_{LOAD}^2 \times R_{DS(ON)1}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often constrains how small the MOSFET can be.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV^2f_{SW} switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, reconsider the MOSFET selection.

Calculating the power dissipation in Q1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation and thermal measurements:

$$PD(Q1\_Switching) = \frac{C_{RSS} \times V_{IN(MAX)}^2 \times f_{SW} \times I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of Q1 and I_{GATE} is the peak gate-drive source/sink current (1.5A typ for BUCK1, 0.75A typ for BUCK2).

For the low-side MOSFET (Q2), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(Q2) = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \times I_{LOAD}^2 \times R_{DS(ON)2}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT(HIGH)} + (LIR/2) \times I_{LOAD(MAX)}$$

where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation.

The MOSFETs must have a good-sized heat sink to handle the overload power dissipation. If short-circuit protection without overload protection is enough, a normal I_{LOAD} value can be used for calculating component stresses.

Choose a Shottky diode (D1) having a forward voltage low enough to prevent the Q2 MOSFET body diode from turning on during the dead time. As a general rule, a diode having a DC current rating equal to 1/3 of the load current is sufficient. This diode is optional and can be removed if efficiency is not critical.

Linear Regulator Design Procedure

Output Voltage Selection

Adjust the linear regulator's output voltage by connecting a resistive voltage-divider from V_{LIN} to AGND with the center tap connected to LINFB (Figure 1). Select R9 in the range of 10kΩ to 100kΩ. Calculate R8 with the following equation:

$$R8 = R9\ [(V_{LIN} / 1.00V) - 1]$$

Pass Transistor Selection

The PNP pass transistor must meet specifications for current gain (h_{FE}), input capacitance, emitter-collector saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = \left(I_{DRV} - \frac{V_{EB}}{R_{EB}}\right) h_{FE(MIN)}$$

where I_{DRV} is the minimum base-drive current, and R_{EB} is the pullup resistor connected between the transistor's emitter and base. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain (see the *Linear Regulator Stability Requirements* section), so excessive gain destabilizes the output. Therefore, transistors with current gain over 300A/A at the maximum output current are not recommended. The transistor's input capacitance and input resistance also create a second pole, which could be low enough to make the output unstable when heavily loaded.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator supports. Alternatively, the package's power dissipation could limit the usable maximum input-to-output voltage differential. The maximum power dissipation capability of the transistor's package and mounting must exceed the actual power dissipation in the device.

The power dissipation equals the maximum load current times the maximum input-to-output voltage differential:

$$P = I_{LOAD(MAX)} \times (V_{LDOIN} - V_{LIN}) = I_{LOAD(MAX)} \times V_{CE}$$

Linear Regulator Stability Requirements

The MAX1816/MAX1994 linear-regulator controller uses an internal transconductance amplifier to drive an external pass transistor. The transconductance amplifier, the pass transistor, the emitter-base resistor, and the output capacitor determine the loop stability. If the output capacitor and pass transistor are not properly selected, the linear regulator is unstable.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. Since the output voltage is a function of the load current and load resistance, the total DC loop gain is approximately:

$$A_{V(LDO)} = \left(\frac{V_{REF}}{V_T}\right)\left[1 + \left(\frac{I_{BIAS} h_{FE}}{I_{LOAD}}\right)\right] 5.5$$

where V_T is 26mV at room temperature, I_{BIAS} is the current though the emitter-base resistor (R_{EB}), and V_{REF} = 1.0V. This bias resistor is typically 220Ω, providing approximately 3.2mA of bias current.

The output capacitor and the load resistance create the dominant pole in the system. However, the pass transistor's input capacitance creates a second pole in the system. Additionally, the output capacitor's ESR generates a zero. To achieve stable operation, use the following equations to verify that the linear regulator is properly compensated:

1) First, determine the dominant pole set by the linear regulator's output capacitor and the load resistor:

$$f_{POLE(CLDO)} = \frac{1}{2\pi C_{LDO} R_{LOAD}} = \frac{I_{LOAD(MAX)}}{2\pi C_{LDO} V_{LDO}}$$

The unity gain crossover of the linear regulator is:

$$f_{CROSSOVER} = A_{V(LDO)} f_{POLE(CLDO)}$$

2) Next, determine the second pole set by the emitter-base capacitance (including the transistor's input capacitance), the transistor's input resistance, and the emitter-base pullup resistor:

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

$$f_{POLE(CEB)} = \frac{1}{2\pi C_{EB}(R_{EB} \parallel R_{IN})} = \frac{R_{EB}I_{LOAD} + V_T h_{FE}}{2\pi C_{EB} R_{EB} V_T h_{FE}}$$

3) A third pole is set by the linear regulator's feedback resistance and the capacitance between LINFB and GND, including the stray capacitance:

$$f_{POLE(FB)} = \frac{1}{2\pi C_{FB}(R8 \parallel R9)}$$

4) If the second and third poles occur well after unity gain crossover, the linear regulator remains stable:

$$f_{POLE(CEB)} > 2f_{POLE(CLDO)}A_{V(LDO)}$$

However, if the ESR zero occurs before the unity gain crossover, cancel the zero with the feedback pole by changing circuit components such that:

$$f_{POLE(FB)} \approx \frac{1}{2\pi C_{LDO} R_{ESR}}$$

For most applications where ceramic capacitors are used, the ESR zero always occurs after the crossover.

Output Capacitor Selection

Typically, more output capacitance provides the best performance, since this also reduces the output voltage drop immediately after a load transient. Connect at least a 10µF capacitor between the linear regulator's output and ground, as close to the external pass transistor as possible. Depending on the selected pass transistor, larger capacitor values may be required for stability (see the *Linear Regulator Stability Requirements* section). Furthermore, the output capacitor's ESR affects stability. Use output capacitors with an ESR less than 200mΩ to ensure stability and optimum transient response. Once the minimum capacitor value for stability is determined, verify that the linear regulator's output does not contain excessive noise. Although adequate for stability, small capacitor values can provide too much bandwidth, making the linear regulator sensitive to noise. Larger capacitor values reduce the bandwidth, thereby reducing the regulator's noise sensitivity.

Applications Information

Voltage Positioning

Powering new mobile processors requires new techniques to reduce cost, size, and power dissipation. Voltage positioning reduces the total number of output capacitors to meet a given transient response requirement. Setting the no-load output voltage slightly higher allows a larger step down when the output current suddenly increases, and regulating at the lower output voltage under load allows a larger step up when the output current suddenly decreases. Allowing a larger step size means that the output capacitance can be reduced and the capacitor's ESR can be increased.

Adding a series output resistor positions the full-load output voltage below the actual DAC programmed voltage. Connect FB directly to the inductor side of the voltage-positioning resistor (R1, 1mΩ). The other side of the voltage-positioning resistor should be connected directly to the output filter capacitor with a short, wide PC board trace. With the gain pin floating (GAIN = 2), a 20A full-load current causes a 40mV drop in the output. This 40mV is a -3.2% droop.

An additional benefit of voltage positioning is reduced power consumption at high load currents. Because the output voltage is lower under load, the CPU draws less current. The result is lower power dissipation in the CPU, although some extra power is dissipated in R1. For a nominal 1.25V, 20A output, reducing the output voltage by 3.2% gives an output voltage of 1.21V and an output current of 19.4A. Given these values, CPU power consumption is reduced from 25W to 23.5W. The additional power consumption of R1 is:

$$1m\Omega \times (19.4A)^2 = 0.38W$$

And the overall power savings is as follows:

$$25W - (23.5W + 0.38W) = 1.12W$$

In effect, 1.5W of CPU dissipation is saved, and the power supply dissipates some of the power savings, but both the net savings and the transfer of dissipation away from the hot CPU are beneficial.

High-Current Master-Slave Applications

The MAX1816/MAX1994 can be used in high-current applications using additional slave regulators. Figure 2 illustrates a 40A master-slave application using this technique. The MAX1994 is placed in forced PWM mode to simplify operation with the slave. Refer to the MAX1980 data sheet for a detailed description of the master-slave architecture and how to configure correctly the slave circuit.

Dropout Performance

The output voltage adjustment range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot (375ns max at 550kHz and 1000kHz). For best dropout performance, use the slower (200kHz) on-time settings.

When working with low-input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K factor. This error is greater at higher frequencies (Table 3).

Also, keep in mind that transient response performance of buck regulators operated close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ is an indicator of ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current is less able to increase during each switching cycle and V_{SAG} greatly increases, unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but this can be adjusted up or down to allow trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \frac{(V_{OUT} + V_{DROP1})}{1 - \left(\frac{T_{OFF(MIN)} \times h}{K}\right)} + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths, respectively (see the *On-Time One-Shot (TON)* section), $T_{OFF(MIN)}$ is from the *Electrical Characteristics* table, and K is taken from Table 3. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then operating frequency must be reduced or output capacitance added to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example

V_{OUT} = 1.2V

f_{SW} = 300kHz

K = 3.3µs, worst-case K = 2.97µs

$T_{OFF(MIN)}$ = 500ns

$V_{DROP1} = V_{DROP2}$ = 100mV

h = 1.5

$$V_{IN(MIN)} = \frac{(1.2V + 0.1V)}{1 - \left(\frac{0.5\mu s \times 1.5}{2.97\mu s}\right)} + 0.1V - 0.1V = 1.74V$$

Calculate again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = \frac{(1.2V + 0.1V)}{1 - \left(\frac{0.5\mu s \times 1}{2.97\mu s}\right)} + 0.1V - 0.1V = 1.56V$$

Since 1.56V is less than the lower limit of the input voltage range (2V), the practical minimum input voltage with reasonable output capacitance would be 2V.

One-Stage (Battery Input) vs. Two-Stage (5V Input) Conversion

The MAX1816/MAX1994 can be used with a direct battery connection (one stage) or can obtain power from a regulated 5V supply (two stage). Each approach has advantages, and careful consideration should go into the selection of the final design.

The one-stage approach offers smaller total inductor size and fewer capacitors overall due to the reduced demands on the 5V supply. The transient response of the single stage is better due to the ability to ramp up the inductor current faster. The total efficiency of a single stage is better than the two-stage approach.

The two-stage approach allows flexible placement due to smaller circuit size and reduced local power dissipation. The power supply can be placed closer to the CPU for better regulation and lower I^2R losses from PC board traces. Although the two-stage design has worse transient response than the single stage, this can be offset by the use of a voltage-positioned converter.

Ceramic Output Capacitor Applications

Ceramic capacitors have advantages and disadvantages. They have ultra-low ESR and are noncombustible, relatively small, and nonpolarized. They are also expensive and brittle, and their ultra-low ESR characteristic can result in excessively high ESR zero frequencies (affecting stability in nonvoltage-positioned circuits). In addition, their relatively low capacitance value can cause output overshoot when going abruptly from full-load to no-load conditions, unless the inductor value can be made small (high switching frequency), or there are some bulk tantalum or electrolytic capacitors in parallel to absorb the stored energy in the inductor. In some cases, there may be no room for electrolytic capacitors, creating a need for a DC-DC design that uses nothing but ceramic capacitors.

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

The MAX1816/MAX1994 can take full advantage of the small size and low ESR of ceramic output capacitors in a voltage-positioned circuit. The addition of the positioning resistor increases the ripple at FB, lowering the effective ESR zero frequency of the ceramic output capacitor.

Output overshoot (V_{SOAR}) determines the minimum output capacitance requirement (see the *Output Capacitor Selection* section). Often the switching frequency is increased to 550kHz or 1000kHz, and the inductor value is reduced to minimize the energy transferred from inductor to capacitor during load-step recovery. The efficiency penalty for operating at 550kHz is about 2% to 3% and about 5% at 1000kHz when compared to the 300kHz voltage-positioned circuit, primarily due to the high-side MOSFET switching losses.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 13). Refer to the MAX1816/MAX1994 EV kit data sheet for a specific layout example.

If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Isolate the power components on the top side from the sensitive analog components on the bottom side with a ground shield. Use a separate PGND plane under the BUCK1 and BUCK2 sides (called PGND1 and PGND2). Avoid the introduction of AC currents into the PGND1 and PGND2 ground planes.
2) Use a star ground connection on the power plane to minimize the crosstalk between BUCK1 and BUCK2.
3) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
4) Connect all analog grounds to a separate solid copper plane, which connects to the AGND pin of the MAX1816/MAX1994. This includes the V_{CC} bypass capacitor, REF bypass capacitor, compensation components, the TIME resistor, as well as any other resistive dividers.
5) Tie AGND and PGND together close to the IC. Do not connect them together anywhere else. Carefully follow the grounding instructions in the *Layout Procedure*.
6) In high-current master-slave applications, the master controller should have a separate analog ground. Return the appropriate noise-sensitive components to this plane. Since the reference in the master is sometimes connected to the slave, it may be necessary to couple the analog ground in the master to the analog ground in the slave to prevent ground offsets. A low value (≤10Ω) resistor is sufficient to link the two grounds.
7) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can enhance full load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
8) Keep the high-current gate-driver traces (DL_, DH_, LX_, and BST_) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
9) CS1+, CS1-, CS2, and AGND connections for current limiting must be made using Kelvin-sense connections to guarantee the current-limit accuracy. Kelvin connections to LX2 and AGND must also be made if the synchronous rectifier $R_{DS(ON)}$ of BUCK2 is used for current limiting. With 8-pin SO MOSFETs, this is best done by routing power to the MOSFETs from the outside using the top copper layer, while connecting GND and LX inside (underneath) the 8-pin SO package.
10) When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
11) Route high-speed switching nodes away from sensitive analog areas (CC, REF, ILIM_). Make all pin-strap control input connections (SKP_/$\overline{SDN}$, ILIM_, etc.) to analog ground or V_{CC} rather than power ground or V_{DD}.

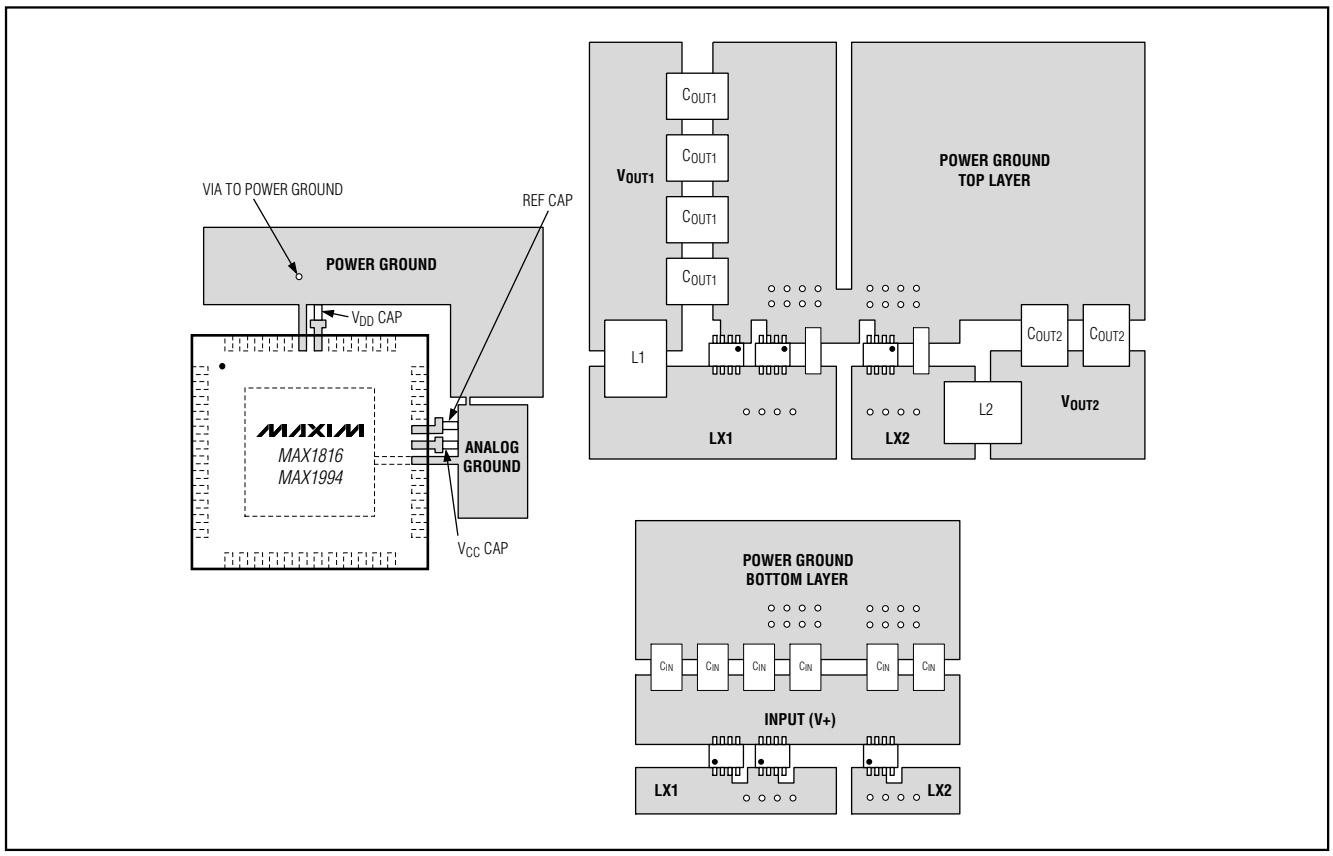


Figure 13. Power-Stage PC Board Layout Example

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET sources, $C_{IN\_}$, $C_{OUT\_}$, D1/D2 anodes). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the backside in order to keep LX_, PGND_, and the DL_ drive lines short and wide. The DL_ gate traces must be short and wide, measuring 10 to 20 squares (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).
3) Group the gate-drive components (BST_ diodes and capacitors, V_{DD} bypass capacitor) together near the controller IC.
4) Make the MAX1816/MAX1994 controllers' ground connections as shown in Figure 13. This diagram can be viewed as having three separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND pin and V_{DD} bypass capacitors go; and an analog ground plane where sensitive analog components go. The analog ground plane and power ground plane must meet only at a single point close to the IC. These two planes are then connected to the high-power output ground with a short connection from PGND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

Chip Information

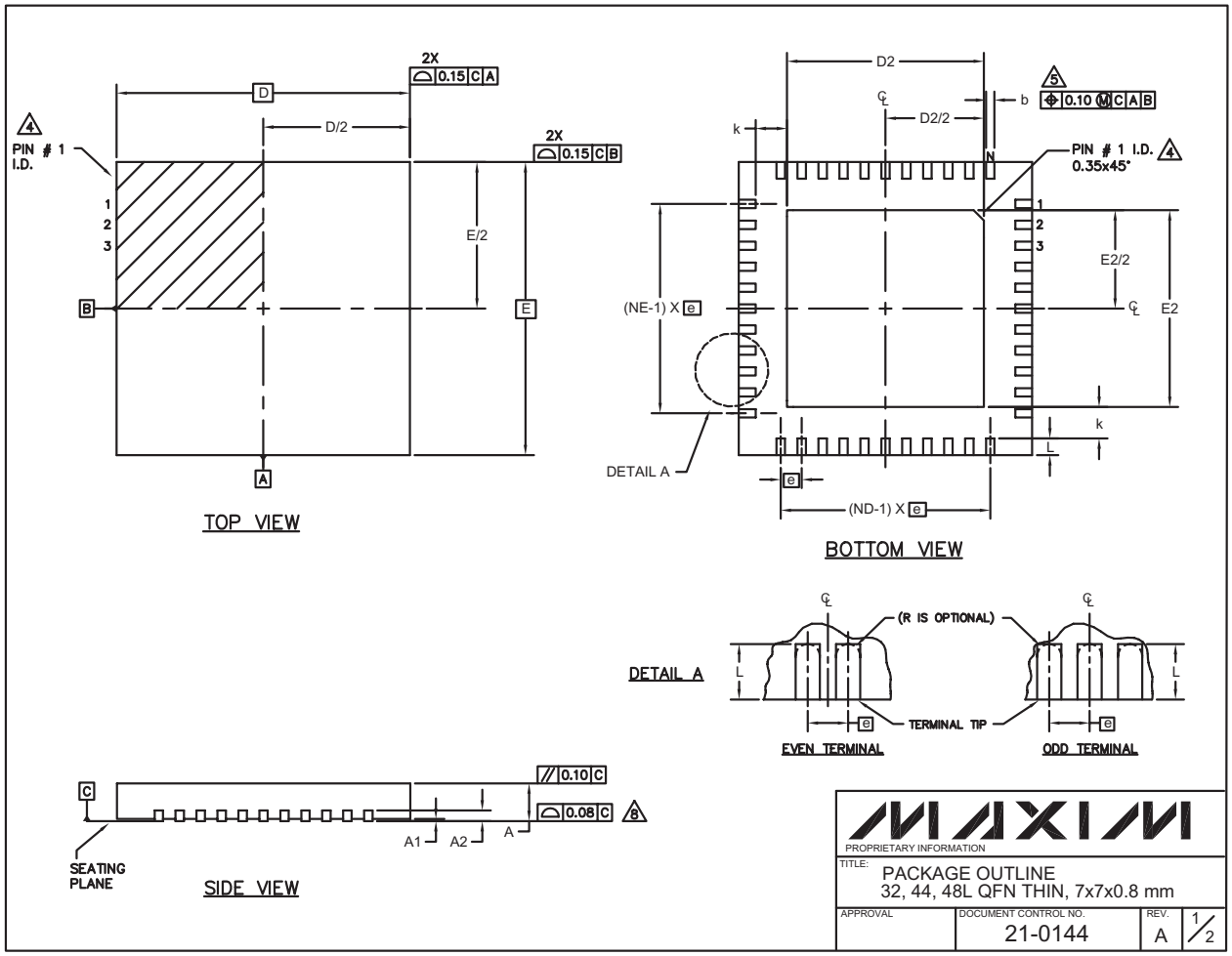
TRANSISTOR COUNT: 13,313

Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN .EPS



Dual Step-Down Controllers Plus Linear-Regulator Controller for Notebook Computers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65
N	32			44			48			44		
ND	8			11			12			10		
NE	8			11			12			12		

EXPOSED PAD VARIATIONS								
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-1	-	4.55	4.70	4.85	4.55	4.70	4.85	-
T4477-1	-	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13, 24, 37, 48	4.20	4.30	4.40	4.20	4.30	4.40	-
T4877-2	-	5.45	5.60	5.75	5.45	5.60	5.75	WKKD-2

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 32, 44, 48L QFN THIN, 7x7x0.8 mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0144	REV. A	2/2